

## **Blue Pearl Software Introduces Debug Environment in Release 9.0**

*Visual Debug and Verification dramatically shortens design cycle time*

**Santa Clara, California** – February 11, 2015 – Blue Pearl Software, Inc., the provider of EDA software that accelerates IP and FPGA verification, announces release 9.0 of its software suite for Windows® and Linux® operating systems. It introduces the new Blue Pearl Debug Environment that significantly reduces the time it takes designers to solidify RTL functionality.

“The Blue Pearl Debug Environment changes the design exploration and debug game by providing functionalities that do not exist with other tools,” said Ellis Smith, Chairman and CEO, Blue Pearl Software. “With release 9.0 we are seeing up to 50% runtime reduction in false path and multi cycle path generation for the largest customer designs”

Release 9.0 of the Blue Pearl Software Suite decreases development time with the new Debug Environment by shrinking the time to find and correct design mistakes. Key features include access to the HDL database once a design is loaded, RTL to schematic cross probe, advanced tracing to specific design elements, hierarchical name search and net coloring across hierarchy for ease of use.

The Debug Environment enhances Blue Pearl’s Visual Verification Environment™ which includes additional time saving debug features of viewing schematic from messages, showing registers on clock paths, waivers capability, graphical representation of FSMs, CDC and false path viewers with cross probing to RTL, schematic representation of RTL with forward and reverse tracing, and linting message filtering.

### **To Learn More**

Release 9.0 of the Blue Pearl Software Suite will be demonstrated at DVCon 2015, Mar 2-5, Booth #1005, Double Tree Hotel, San Jose, California.

## **Availability**

General availability of Release 9.0 of the Blue Pearl Software Suite will be early March 2015.

Please contact [sales@bluepearlsoftware.com](mailto:sales@bluepearlsoftware.com) to arrange a demo, or for additional pricing and upgrade information.

## **About Blue Pearl Software**

[Blue Pearl Software, Inc.](#) provides EDA software that accelerates FPGA design verification. The company's [Blue Pearl Software Suite](#) checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA design risks.

Visit Blue Pearl Software at <http://www.bluepearlsoftware.com>.

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