Blue Pearl Software Suite Customized for Xilinx Users

Xilinx design methodology checklist implemented within the Blue Pearl Software Suite

Santa Clara, California – June 03, 2013 -- Blue Pearl Software, the provider of EDA software that accelerates FPGA design verification, today announced the availability of a customized version of its software suite that implements the Xilinx design methodology checklist. Xilinx users can now verify their RTL for issues that are traditionally found late in the design cycle.

As FPGA designs increase in complexity, debugging in the lab is unrealistic. Not only it is too late, but it is a very costly proposition. Some of the design issues that traditionally have been found after synthesis or simulation can be identified earlier by using RTL analysis tools like the Blue Pearl Software Suite.

"Xilinx's 7 Series All Programmable FPGAs and SoCs deliver breakout performance, capacity, and system integration to address the needs of today's smarter systems," said Tom Feist, senior marketing director of design methodology at Xilinx. "As design complexity has increased, so too has the need for advanced design methodologies. Our close collaboration with Blue Pearl Software has resulted in a solution that can significantly reduce our mutual customers design iterations, verification and debug time, enabling them to get their products to market faster."

"Blue Pearl Software is all about reducing risk by enabling FPGA verification early in the design cycle" noted Ellis Smith, Chairman and CEO, Blue Pearl Software. "By supplementing our tools with the Xilinx design methodology checklist, we are enabling FPGA designers to start the verification process right from their RTL."

The Blue Pearl Software Suite works with the Xilinx Vivado Design Suite running on Windows platforms. It includes linting, CDC analysis and automatic SDC generation. Its generated SDCs drive the efficiency of the synthesis and place and route phases of FPGA design implementation, and reduce iterations and overall design time. Its Visual Verification Environment™ makes it easy to use.

The company's collaboration with Mentor Graphics and Synopsys offers an optimized flow that works with Precision and Synplify Pro FPGA synthesis software. Verilog, VHDL and SystemVerilog designers can automatically generate an exhaustive set of constraints that address false and multi-cycle paths that are compatible with Synopsys' synthesis flow.

About Blue Pearl Software

Blue Pearl Software, Inc. provides EDA software that accelerates FPGA design verification. The company's Blue Pearl Software Suite checks RTL designs for functional errors and automatically generates comprehensive

and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA design risks.

Visit Blue Pearl Software at http://www.bluepearlsoftware.com.

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