



Blue Pearl Software

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Blue Pearl Software Opens Japan Office and Appoints Katsuhiko Sakano as Sales Director to Support Growing Interest in FPGA Design Tools for Embedded Applications

SANTA CLARA, CA and TOKYO--(Marketwire - Dec 13, 2012-- [Blue Pearl Software](#), the provider of EDA software that accelerates RTL signoff for FPGA designs, today announced it has opened a Japan office in Tokyo, and appointed [Katsuhiko Sakano](#) as its Director of Sales.

“By opening this office and adding an experienced executive like Sakano to our management team, we continue to support our growing list of Japanese FPGA designers,” said Ellis Smith, Blue Pearl’s CEO.

“We are dedicated to providing FPGA designers in Japan with the best design tools for their innovative embedded systems and quality electronic products,” noted Sakano. “The [Blue Pearl Software Suite](#) runs on Windows, is easy to use, and is priced right. It also accelerates RTL signoff, supports SystemVerilog, and works with FPGA design flows supported by Xilinx and Synopsys.”

[Sakano](#) is an experienced EDA sales executive, who previously worked with Real Intent, Inc. and Springsoft K. K. (now part of Synopsys, Inc.), as well as Cadence Design Systems and leading semiconductor and FPGA companies.

Japan Contact Information for Blue Pearl Software

Blue Pearl Software
Shinjuku Nomura Building, Tokyo
Level 32, Shinjuku Nomura Building
1-26-2 Nishi-Shinjuku, Shinjuku-ku
Tokyo, Japan 163-0532
Tel: +81 3 5322 2856
ksakano@bluepearlsoftware.com

About the Blue Pearl Software Suite for FPGA RTL Signoff

The [Blue Pearl Software Suite](#) works with the Xilinx Vivado Design Suite running on Windows platforms. It includes linting, CDC analysis and automatic SDC generation. Its generated SDCs drive the efficiency of the synthesis and place and route phases of FPGA design implementation, and reduce iterations and overall design time. Its Visual Verification Environment™ makes it easy to use.

The company’s collaboration with Synopsys offers an optimized flow that works with Synopsys’ Synplify Pro FPGA synthesis software. Verilog, VHDL and SystemVerilog designers can automatically generate an

exhaustive set of constraints that address false and multi-cycle paths that are compatible with Synopsys' synthesis flow.

About Blue Pearl Software

[Blue Pearl Software, Inc.](#) provides EDA software that accelerates RTL signoff for FPGA designs. The company's [Blue Pearl Software Suite](#) checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA design risks.

Visit Blue Pearl Software at <http://www.bluepearlsoftware.com>.

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Press Contact:

Georgia Marszalek, ValleyPR LLC for Blue Pearl Software, +1-650.345.7477, Georgia@ValleyPR.com

Acronyms

CDC: Clock Domain Crossing
EDA: Electronic Design Automation
FPGA: Field Programmable Gate Array
QoR: Quality of Results
RTL: Register Transfer Level
SDC: Synopsys Design Constraints
SoC: System-on-Chip

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