



## Blue Pearl Announces Expansion in China

*Supports Growing Demand for RTL Signoff Software for FPGA Design*

SANTA CLARA, CA--(PRWEB – Feb 07, 2013) -- [Blue Pearl Software](#), the provider of EDA software that accelerates RTL signoff for FPGA designs, today announced the addition of Beijing Hontak Technologies as a distributor in China. Hontak complements Maojet Tech, Blue Pearl’s current distributor in Eastern China.

This expansion is an important milestone in establishing FPGA market leadership for [Blue Pearl Software](#) in Asia-Pacific. As a fast growth region, and one in high demand for innovative FPGA design software, [Blue Pearl Software](#) is increasing its footprint in China.

“By adding experienced distributors to our existing teams of direct sales and distributor channels, we are committed to provide dedicated support to our growing FPGA customers” remarked Ellis Smith, Blue Pearl Software CEO.



To contact Blue Pearl Software’s sales and support offices, please visit

<http://www.bluepearlsoftware.com/company/contact/>

## About the Blue Pearl Software Suite for FPGA RTL Signoff

The [Blue Pearl Software Suite](#) works with the Xilinx Vivado Design Suite running on Windows platforms. It includes linting, CDC analysis and automatic SDC generation. Its generated SDCs drive the efficiency of the synthesis and place and route phases of FPGA design implementation, and reduce iterations and overall design time. Its Visual Verification Environment™ makes it easy to use.

The company's collaboration with Synopsys offers an optimized flow that works with Synopsys' Synplify Pro FPGA synthesis software. Verilog, VHDL and SystemVerilog designers can automatically generate an exhaustive set of constraints that address false and multi-cycle paths that are compatible with Synopsys' synthesis flow.

## About Blue Pearl Software

[Blue Pearl Software, Inc.](#) provides EDA software that accelerates RTL signoff for FPGA designs to improve quality of results (QoR) and reduce FPGA design risks. The [Blue Pearl Software Suite](#) finds and analyzes the longest path using the RTL design (rather than the netlist), generates SDCs automatically for false and multi-cycle paths, enables full-chip CDC analysis by improving inter-IP analysis using its Grey Cell methodology, and determines the number of logic levels in a design to analyze resource usage for best fit into the target FPGA.

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### Acronyms

CDC: Clock Domain Crossing  
EDA: Electronic Design Automation  
FPGA: Field Programmable Gate Array  
QoR: Quality of Results  
RTL: Register Transfer Level  
SDC: Synopsys Design Constraints  
SoC: System-on-Chip

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