

Blue Pearl Software Appoints Murielle Lacomblet as Sales Director, Southern Europe to Support the Growing Demand for FPGA Design Tools

Santa Clara, California and Paris, France – April 30 -- [Blue Pearl Software](#), the provider of EDA software that accelerates RTL signoff for FPGA designs, today announced it has appointed Murielle Lacomblet as its Director of Sales for Southern Europe.

“By adding an experienced FPGA professional like Murielle to Southern Europe, we enhance support for our growing list of European customers, who design with FPGAs and are using them for embedded applications,” said Roger Bitter, Vice President Worldwide Sales, Blue Pearl Software. “Our customers will benefit from her responsiveness and excellent business abilities.”

“We are dedicated to providing the leading electronic and semiconductor companies in Europe with the most advanced design tools for their innovative electronic products,” noted Murielle Lacomblet. “The Blue Pearl Software technology brings a unique ASIC-like verification approach to FPGA designers at the RTL level, and thus boosts design verification productivity in major FPGA design flows.”

Murielle is experienced in international sales for Electronic Design Automation (EDA), and previously worked for Cavium, MontaVista, Synplicity, as well as Cadence Design Systems.

The [Blue Pearl Software Suite](#) works with the Xilinx Vivado Design Suite running on Windows platforms. It includes linting, CDC analysis and automatic SDC generation. Its generated SDCs drive the efficiency of the synthesis and place and route phases of FPGA design implementation, and reduce iterations and overall design time. Its Visual Verification Environment™ makes it easy to use.

The company’s collaboration with Synopsys offers an optimized flow that works with Synopsys’ Synplify Pro FPGA synthesis software. Verilog, VHDL and SystemVerilog designers can automatically generate an exhaustive set of constraints that address false and multi-cycle paths that are compatible with Synopsys’ synthesis flow.

About Blue Pearl Software

[Blue Pearl Software, Inc.](#) provides EDA software that accelerates RTL signoff for FPGA designs. The company’s [Blue Pearl Software Suite](#) checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA design risks.

Visit Blue Pearl Software at <http://www.bluepearlsoftware.com>.

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Acronyms

CDC: Clock Domain Crossing
EDA: Electronic Design Automation
FPGA: Field Programmable Gate Array
QoR: Quality of Results
RTL: Register Transfer Level
SDC: Synopsys Design Constraints
SoC: System-on-Chip

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