

Blue Pearl Software Joins Mentor OpenDoor Program

Santa Clara, California – May 21-- [Blue Pearl Software](#), the provider of EDA software that accelerates FPGA verification, today announced it has joined the OpenDoor program of Mentor Graphics.

“Mentor Graphics strongly believes that EDA providers need to ensure a smooth data flow between their tools,” said Rajeev Sehgal, Product Line Director for Precision Synthesis, Mentor Graphics Corporation “Our collaboration with Blue Pearl Software will minimize the customer’s FPGA design flow iterations and increase early design productivity to help meet their time-sensitive product schedules.”

Blue Pearl Software’s collaboration with Mentor Graphics offers an optimized flow that works with Mentor’s Precision Synthesis software. Verilog, VHDL and SystemVerilog designers can automatically generate an exhaustive set of constraints that address false and multi-cycle paths that are compatible with Mentor’s synthesis flow. With a rich feature set that includes advanced optimizations, award-winning analysis, and industry-leading language support, Mentor’s Precision Synthesis product enables vendor-independent design, accelerates time to market, and delivers superior quality of results.

“As our customer base grows we are seeing increasing demand for powerful FPGA synthesis tools,” noted Shakeel Jeeawoody, Vice President Marketing, Blue Pearl Software. “The Blue Pearl Software technology automates a critical and time-consuming aspect of timing closure and this collaboration with Mentor Graphics will boost design productivity in major FPGA design flows.”

The [Blue Pearl Software Suite](#) works with the Xilinx Vivado Design Suite running on Windows platforms. It includes linting, CDC analysis and automatic SDC generation. Its generated SDCs drive the efficiency of the synthesis and place and route phases of FPGA design implementation, and reduce iterations and overall design time. Its Visual Verification Environment™ makes it easy to use.

About Blue Pearl Software

[Blue Pearl Software, Inc.](#) provides EDA software that accelerates RTL signoff for FPGA designs. The company’s [Blue Pearl Software Suite](#) checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA design risks.

Visit Blue Pearl Software at <http://www.bluepearlsoftware.com>.

###

Press Contact:

Shakeel Jeeawoody, Blue Pearl Software, +1- 408.961.0121, shakeel@bluepearlsoftware.com