Blue Pearl Software Advances FPGA RTL Signoff, Announces Release 6.2 with Enhanced Grey Cell Methodology

Demos set for Embedded World, Feb 26-28, 2013, Nuremberg, Germany

SAN JOSE, Calif.(BUSINESS WIRE) -February 20 2013 -Blue Pearl Software, Inc, the provider of next generation EDA software that increases designer productivity and design quality, announced that it is shipping Release 6.2 of its Blue Pearl Software Suite, for Windows and Linux operating systems. The new version includes enhancements that improve and further accelerates FPGA design verification, including one of its biggest design challenges – chip-level clock domain crossing analysis.

"We are very pleased to see that the Blue Pearl Software Suite integrates well with Xilinx's latest solutions like Vivado™ Design Suite and Zynq™-7000 All Programmable SoC, said Sanjay Gehani, Senior Manager Alliance Program at Xilinx. This addresses the growing verification concerns of IP connectivity and rule compliance checking for complex FPGAs."

"Our collaboration with Xilinx resulted in an optimized flow for the FPGA synthesis and place & route implementation flow," said Ellis Smith, Chairman and CEO of Blue Pearl. "With our enhanced Grey Cell methodology we are now enabling an industry-first chip-level clock-domain crossing (CDC) solution at the RTL level."

What's New in 6.2

Enhancements to Blue Pearl Software Suite™ Version 6.2 include:

- Enhanced analysis using a Grey Cell methodology
- Better runtime due to enhanced connectivity and smaller database
- Enhanced multi-cycle path analysis

Previous announcements included multi-language (SystemVerilog, VHDL, and Verilog) support, mode-based path analysis, TCL tool control, a longest path viewer and an improved FPGA synthesis flow.

What's our Grey Cell methodology

Blue Pearl's Grey Cell methodology allows design modules to be represented as Grey Cells which exclude all register-to-register logic. Grey Cells contain only all logic from each input up to and including the nearest register, and all logic from each output back to and including the nearest register. Grey cells enable the analysis of module-to-module connections while making abstraction of the details and/or preserving the trade secrets of the original IP provider.

About the Blue Pearl Software Suite for FPGA RTL Signoff

The Blue Pearl Software Suite works with the Xilinx Vivado Design Suite running on Windows platforms. It includes linting, CDC analysis and automatic SDC generation. Its generated SDCs drives the effectiveness of synthesis and place and route phases of FPGA design implementation, and reduce iterations and overall design time. Its Visual Verification Environment™ makes it easy to use.

The company's collaboration with Synopsys offers an optimized flow that works with Synopsys' Synplify Pro FPGA synthesis software. Verilog, VHDL and SystemVerilog designers can automatically generate an exhaustive set of constraints that address false and multi-cycle paths that are compatible with Synopsys' synthesis flow.

To Learn More

Blue Pearl Software Suite will be demonstrated at Embedded World 2013, Hall 4-615, NürnbergMesse, Nuremberg, Germany.

Please click on the following links to sign up for a hands-on workshops and software evaluations.

Price and Availability

Release 6.2 of Blue Pearl Software Suite is available now. Please contact sales@bluepearlsoftware.com to arrange a demo or for pricing and upgrade information.

About Blue Pearl Software

Blue Pearl Software, Inc. provides RTL Signoff software that uses new and innovative technology to reduce design flow iterations and increase designer productivity early in the digital design flow. By partnering with key players of the FPGA Ecosystem, Blue Pearl Software accelerates FPGA implementation. Blue Pearl Software Suite checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA and ASIC design risks.

Visit Blue Pearl Software at http://www.bluepearlsoftware.com.

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Press Contact:
Shakeel Jeeawoody, Blue Pearl Software, +1- 408.961.0121, shakeel@bluepearlsoftware.com

Acronyms

ASIC:	Application Specific Integrated Circuit
CDC:	Clock Domain Crossing
EDA:	Electronic Design Automation
FPGA:	Field Programmable Gate Array
RTL:	Register Transfer Level
SDC:	Synopsis Design Constraints
SOC:	System on Chip
Tcl:	Tool Command Language