

Blue Pearl Software Adds STARC Support to further FPGA RTL Signoff

Demos set for DATE, March 19-21, 2013, Grenoble, France

SAN JOSE, Calif. -March 13, 2013 -**Blue Pearl Software, Inc**, the provider of next generation EDA software that increases designer productivity and design quality, announced that it has added support of STARC (Semiconductor Technology Academic Research Center) to its Blue Pearl Software Suite, for Windows and Linux operating systems. Designers can now perform RTL analysis and ensure compliance with best practices and reuse guidelines based on the STARC rules.

“Our customers who trust the STARC rules can now verify their designs using the STARC package within the Blue Pearl Software Suite, said Katsuhiko Sakano, Director of Japan Sales, Blue Pearl Software. We continue to make it easier for designers of complex FPGAs to verify connectivity and rule compliance.”

The Blue Pearl Software Suite already includes multiple packages that incorporate best design practices, namely the Reuse Methodology Manual, Semiconductor Reuse Manual, Simulation and Synthesis checks. In addition, users of the Blue Pearl Software Suite can add their own checks as the need arise.

About the Blue Pearl Software Suite for FPGA RTL Signoff

The Blue Pearl Software Suite works with the Xilinx Vivado Design Suite running on Windows platforms. It includes linting, CDC analysis and automatic SDC generation. Its generated SDCs drive the effectiveness of synthesis and place and route phases of FPGA design implementation, and reduce iterations and overall design time. Its Visual Verification Environment™ makes it easy to use.

The company’s collaboration with Synopsys offers an optimized flow that works with Synopsys’ Synplify Pro FPGA synthesis software. Verilog, VHDL and SystemVerilog designers can automatically generate an exhaustive set of constraints that address false and multi-cycle paths that are compatible with Synopsys’ synthesis flow.

To Learn More

Blue Pearl Software Suite will be demonstrated at DATE 2013, March 19-21, Grenoble, France. Please click on the following links to sign up for a hands-on workshops and software evaluations.

Price and Availability

Release 6.2 of Blue Pearl Software Suite is available now. Please contact sales@bluepearlsoftware.com to arrange a demo or for pricing and upgrade information.

About Blue Pearl Software

Blue Pearl Software, Inc. provides RTL Signoff software that uses new and innovative technology to reduce design flow iterations and increase designer productivity early in the digital design flow. By partnering with key players of the FPGA Ecosystem, Blue Pearl Software accelerates FPGA implementation. Blue Pearl Software Suite checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA and ASIC design risks.

Visit Blue Pearl Software at <http://www.bluepearlsoftware.com>.

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Acronyms

ASIC: Application Specific Integrated Circuit
CDC: Clock Domain Crossing
EDA: Electronic Design Automation
FPGA: Field Programmable Gate Array
RTL: Register Transfer Level
SDC: Synopsys Design Constraints
SOC: System on Chip
Tcl: Tool Command Language

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