Blue Pearl Software

Azure

Automatic Timing Constraint Validation

Blue Pearl Software provides innovative solutions that address the most time consuming aspects of closing timing for nanometer technology designs – generating and validating false and multi-cycle path timing exceptions from the register transfer level (RTL) description.

Blue Pearl Software's **Azure** Timing Constraint Validation™ tool uses a combination of high performance breakthrough technologies in state-space search and RTL analysis to perform automatic validation of specified timing exception constraints at the block or chip level. Valid constraints for timing exceptions are vital to reduce design risk and to achieve a high quality of results (QoR).

Main Features

- *Accepts industry standard design and constraint files (Verilog, SDC)*
- *Validates defined false paths*
- *Validates multi-cycle paths*
- *Automatically generates a Verilog test bench for violated constraints*

Benefits

- *Lowers risks in designing chips*
- *Achieves higher quality of results (QoR)*
- *Increases designer productivity*
- *Provides independent verification of violated constraints*

Accurate timing exceptions vital for synthesis design flow

The ASIC and FPGA synthesis design flows are driven by an RTL description and design constraints. The constraints contain implementation directives in a number of areas including clocking, timing and power. Synthesis and place and route implementation tools use these constraints to achieve a design that meets specification.

The majority of timing constraints in the constraints file tend to be false and multi-cycle path exceptions to timing. These timing exceptions reduce the burden on the implementation tools in achieving chip performance targets. Without timing exceptions, chip performance is over constrained. It is very critical to have a correct set of constraints to drive the synthesis design flow efficiently and effectively as flawed constraints can result in an increased number of iterations or even silicon re-spins.

The complex designs being implemented today contain many false path and multi-cycle path timing exceptions. Validation of constraints is a very time-consuming and difficult task that

results in designers spending a lot of manual effort in checking the consistency of the constraints with the design and in writing test-benches. As design complexities increase, design reuse is growing in popularity. The increasing use of IP and legacy design blocks exacerbates the validation problem. Chip designers are usually unfamiliar with the timing exception constraints that are provided with intellectual property (IP) and legacy blocks.

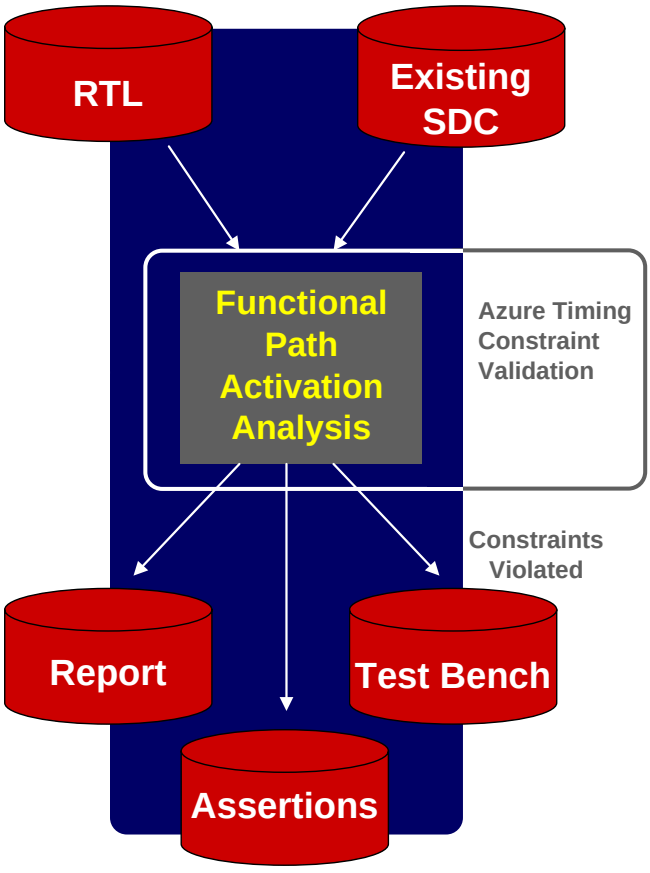
Blue Pearl's **Azure** Automatic Timing Validation solution allows you to check your timing exception constraints rapidly and easily. The more complete the set of constraints are at RTL, the lower your risks and the higher your design productivity.

Azure Automatic Timing Constraint Validation is easy to use in any ASIC or FPGA design flow. The tool accepts Verilog RTL and can read industry standard constraint file formats such as Synopsys Design Constraints (SDC). The tool rapidly analyzes full-chip designs. The timing constraint validation tool performs functional path activation analysis to validate defined timing exceptions such as false and multi-cycle paths in the design. Azure generates an assertion for a valid timing exception constraint.

Existing specifications of false and multi-cycle paths that are found to be incorrect are identified and a counter example, comprising a test bench, is generated. You can use this test-bench for independent verification that the constraint is incorrect using your golden simulator.

Using Blue Pearl Software's **Azure** Automatic Timing Constraint Validation solution considerably enhances your confidence that specified timing exception constraints are valid, improves your design productivity and reduces your design risk.

Improve your productivity in digital design flows with validated timing constraints



Automatic Timing Constraint Validation Flow

Blue Pearl's **Azure** Automatic Timing Constraint Validation tool accepts and outputs industry standard formats for easy integration in digital chip design flows. The Automated Timing Constraint Validation tool alleviates manual checking of exceptions and associated risks.

The high performance breakthrough technology allows very fast validation of timing exception constraints for very large designs from the RTL description. Validating timing constraints with this tool provides you with a lower risk faster.

Language Support
Verilog 2001

Platform Support
Unix/Solaris, Windows XP/2000, & Linux

Blue Pearl Software, Inc. ■ 4677 Old Ironsides Dr. #430 ■ Santa Clara, CA 95054
Phone: 408.961.0121 ■ Fax: 408.961.0125 ■ info@bluepearlsoftware.com
www.bluepearlsoftware.com