Blue Pearl Software

Cobalt Automatic Timing Constraint Generation

Blue Pearl Software provides innovative solutions that address the most time consuming aspects of closing timing for nanometer technology designs – identifying false and multi-cycle paths and generating timing exceptions from the register transfer level (RTL) description *automatically*.

Blue Pearl Software's **Cobalt** Timing Constraint Generation™ tool uses a combination of high performance breakthrough technologies in symbolic simulation, state-space search and RTL analysis to automatically generate a comprehensive set of timing exceptions. The automatic generation of timing exceptions allows significant reductions in design cycle times in the ASIC and FPGA synthesis flow.

Using **Cobalt**, you can automatically generate high quality timing exceptions that reduce the burden on downstream synthesis and place & route tools, resulting in higher productivity, fewer iterations, and enhanced quality of results (QoR), while also reducing the risks associated with manual generation of timing constraints.

Main Features

- *Automatically identifies false paths*
- *Automatically identifies multi-cycle paths*
- *Supports industry standards for easy integration into design flows*
- *High performance allows full-chip analysis*
- *Generates constraint files in SDC format*
- *Generates assertions in standard formats such as PSL and SVA*

Benefits

- *Automatic generation of timing exceptions results in fewer design iterations and reduced risk*
- *Increase in designer productivity, resulting in reduced design cycle times*
- *Higher quality of results*
- *Independent validation of timing exceptions with automated generation of assertions*

Timing exceptions improve productivity in synthesis design flow

Closing timing for today's increasingly complex designs is an extremely time-consuming and iterative process that involves analyzing timing analysis results after synthesis and identifying false and multi-cycle path exceptions to timing in reported critical paths. In addition to the difficulty of manually identifying timing exceptions, the increasing use of intellectual property (IP) cores and legacy blocks complicates the task. The result is that the timing exceptions for such logic blocks may be incomplete or inaccurate. This leads to over constrained designs, resulting in wasted time and poor synthesis and place and route (P&R) results, or even worse, designs that fail to meet timing.

In a typical RTL design flow the designer creates a functional description of the design in RTL and an initial timing constraint file described in a format, such as the Synopsys Design Constraint (SDC) format. The design consists of blocks that are synthesized into a specific technology. Typically, the designer iteratively refines the constraints to add false and multi-cycle path timing exceptions. After synthesis and timing analysis results are acceptable, further iterations of timing exception generation are performed during the place and route process. These iterations consume additional time as the design has to be synthesized again. It is imperative that timing, functionality, power and area constraints are met throughout the layout process.

The majority of the iterations in the design flow are caused by the manual effort needed to achieve timing closure and the failure to identify all timing constraint issues results in an increased number of synthesis iterations, longer design times and even silicon re-spins.

By using Blue Pearl Software's **Cobalt** Timing Constraint Generation tool to automatically generate a comprehensive set of timing exception constraints, you can significantly improve your design productivity, increase the quality of silicon (QoS) and drastically reduce design flow iterations and the risk of re-spins.

Cobalt Automatic Timing Constraint Generation tool flow

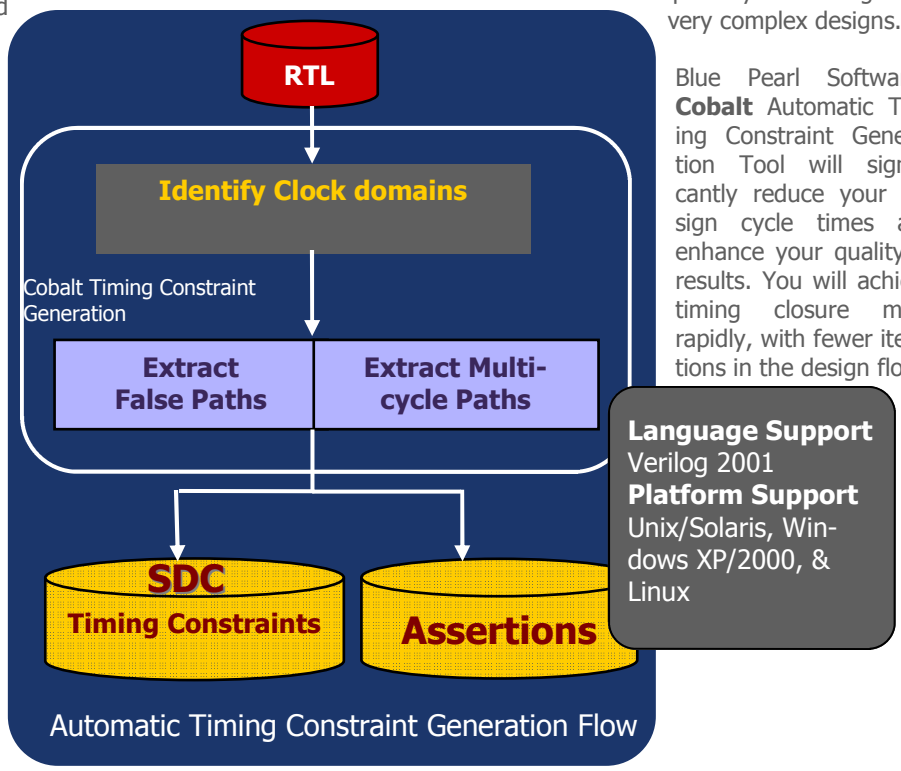
Blue Pearl's **Cobalt** Automatic Timing Constraint Generation tool is very easy to use in any ASIC or FPGA design flow. The tool accepts Verilog RTL and can read industry standard constraint files such as SDC. Blue Pearl's blazingly high performance allows you to analyze your design at the full chip level to provide a comprehensive set of false and multi-cycle paths.

Cobalt performs an analysis of the RTL, identifies all clock domains in the design and creates a clock constraint template for each identified clock in the generated timing constraint file.

Blue Pearl's innovative RTL analysis technology uses a high performance symbolic simulation engine to identify every signal that crosses from one clock domain to another and warns you if synchronization is not properly implemented. Using the generated reports, you can identify and resolve clock synchronization issues in your design early in the design process.

Blue Pearl then automatically identifies false and multi-cycle paths using innovative register transfer level symbolic simulation and state space search technology that allows very high performance analysis of finite state machines (FSMs).

Blue Pearl then generates an SDC file containing a comprehensive set of timing exception constraints. These constraints can be used to drive the synthesis and physical design flow more productively.



Language Support
Verilog 2001
Platform Support
Unix/Solaris, Windows XP/2000, & Linux

You can validate the automatically generated constraints using Blue Pearl's **Azure** Timing Constraint Validation software or external simulation and formal property checking tools. To facilitate validation using your golden simulator or formal verification tool, Blue Pearl produces assertions in industry standard formats such as PSL (Property Specification Language) and SVA (SystemVerilog Assertions). Validating the automatically generated assertions using simulation or formal verification allows you to improve your overall confidence in the timing constraints.

Increase design productivity with automatically generated timing exceptions

Blue Pearl's proprietary and breakthrough symbolic simulation and state space search technologies have been optimized to operate directly at the register transfer level so that you can perform fast and accurate full-chip analysis for large and very complex designs.

Blue Pearl Software's **Cobalt** Automatic Timing Constraint Generation Tool will significantly reduce your design cycle times and enhance your quality of results. You will achieve timing closure more rapidly, with fewer iterations in the design flow.

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