Blue Pearl Software
ASIC, FPGA and IP Verification

Advanced Clock Enviroment (ACE)

Overview

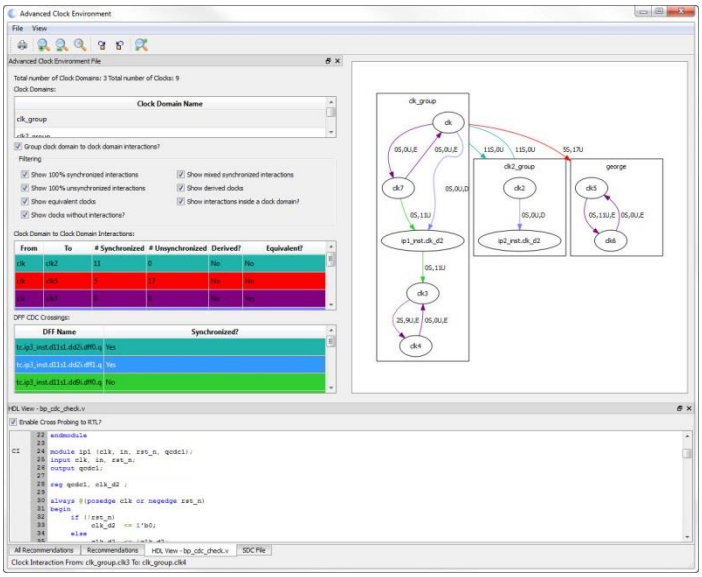
The Blue Pearl Software's Visual Verification Suite is the next generation EDA solution for ASIC, IP and FPGA verification that automates RTL analysis, CDC analysis, and SDC generation.

The Suite augments existing EDA and FPGA vendor tool flows with a native Windows or Linux user experience.

The Advanced Clock Environment (ACE) tool solves the iterative and reactive CDC setup problem experienced by designers. It is used before running a CDC analysis. With ACE, designers can clearly see if clocks are not in the intended domains and make corrections before in-depth CDC analysis.

What is ACE?

Blue Pearl Software's Advanced Clock Environment provides a graphical representation summarizing data paths between clocks and can make recommendations for grouping of clocks into clock domains. With ACE, designers can identify clocks to better understand how they interact with synchronizers in the design. This allows users to quickly identify improper synchronizers or clock domain groupings that cause CDC metastability.



Why should I be concerned with metastability and CDC?

At its most basic level, metastability is what happens within a register when data changes too soon before or after the active clock edge; that is, when setup or hold times are violated. A register in a metastable state is in between valid logic states, and the process of settling to a valid logic state takes much longer than normal. It will eventually fall into a stable "1" or "0" state, but there is no way to predict which way it will fall or how long it will take. If the metastable state lasts longer than one clock cycle, it can be transferred to the next register.

When data is transferred between two registers whose clocks are asynchronous, metastability will happen. There is no way to prevent it. All you can do is to minimize its impact by placing the two clocks in different clock domains and using a clock synchronization technique at the crossing point. Hence the name "clock domain crossing" (CDC).

Putting two clocks into the same clock domain is a declaration that these two clocks are synchronous to each other, and CDCs between them do not need to be synchronized. If the clocks are from the same source, or one is derived from the other, then they are synchronous and should be placed into the same clock domain.

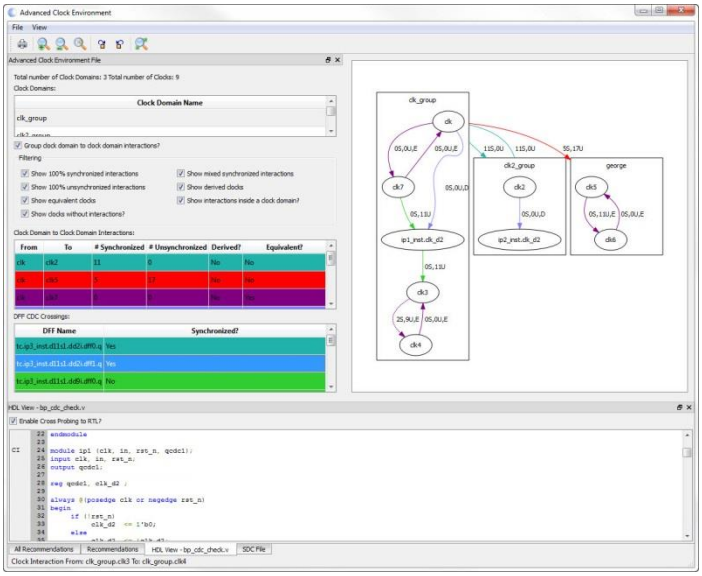
Clocks that are asynchronous to one another should always be placed in different clock domains, and any CDCs between them should be synchronized. Even two clocks of the same frequency should be placed into different domains if they come from independent sources. All specifications have tolerances or "error bars," and two independent clock sources of the same frequency will drift relative to one another over time. Failing to synchronize CDCs between two such clocks will cause metastability problems.

What can I do with ACE?

- Evaluate clock domain definitions
- Evaluate SDC clock constraints
- Generate a graphical analysis of clock and clock domains
- Validate clock grouping recommendations
- Generate SDC template to be used by a CDC analysis tool

Features of ACE

- Detailed analysis of clock, clock groupings, and interactions
- Visual display filters enable quick debug
- Pinpoint exact location of problem in RTL design



Why should I use ACE?

- Without proper clock domain setup, CDC analysis results are unreliable.
- Virtually impossible for any tool to automatically deduce all the clock domains
- Designers perform many CDC iterations as they incrementally make clock / clock domain decisions

The overall goal of Advanced Clock Environment is to enable engineers to find metastability issues in designs by properly grouping clocks into clock domains. Design and Verification engineers use ACE to ensure the clock domains are properly specified before running a CDC analysis.

ACE will quickly find errors in clock domain groupings or find/recommend appropriate clock domain groupings for a circuit that is synchronized.

Engineers who are interested in reducing cycle times, by identifying problems early on, find Blue Pearl's Advanced Clock Environment a great addition to their existing design environment.

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