Blue Pearl Software
ASIC, FPGA and IP Verification

Analyze RTL

Overview

The Blue Pearl Software Visual Verification Suite provides enhanced Lint, Debug, Clock Domain Crossing (CDC) and automated SDC generation flows to accelerate RTL Verification. Analyze RTL™ provides RTL linting combined with a powerful debug environment with the industry's fastest bug find/fix rate to quickly identify critical design issues, up front, streamlining simulation and synthesis while improving overall quality of results.

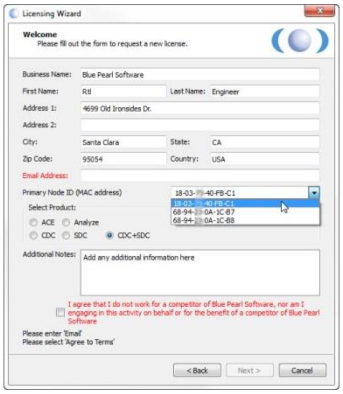
Key Benefits

Modern ASICs, SoCs and FPGAs routinely have millions of gates with memories, transceivers, third party IP and processor cores. RTL issues can be time consuming and complex to debug in the lab and through simulations. To reduce verification and debug times, designers need tools that can identify problems quickly before simulation and synthesis, and definitely before spending time in the lab.

Key Features

Analyze RTL, accelerates RTL verification and debug:

- Fast and meaningful results with tool Setup Wizard



Welcome
Please fill out the form to request a new license.

Business Name:	Blue Pearl Software		
First Name:	Rtl	Last Name:	Engineer
Address 1:	4699 Old Ironsides Dr.		
Address 2:			
City:	Santa Clara	State:	CA
Zip Code:	95054	Country:	USA
Email Address:			

Primary Node ID (MAC address) 18-03-[redacted]-40-FB-C1
18-03-[redacted]-40-FB-C1
68-94-[redacted]-0A-1C-B7
68-94-[redacted]-0A-1C-B8

Select Product:
○ ACE ○ Analyze
○ CDC ○ SDC ● CDC+SDC

Additional Notes: Add any additional information here

□ I agree that I do not work for a competitor of Blue Pearl Software, nor am I engaging in this activity on behalf or for the benefit of a competitor of Blue Pearl Software

Please enter 'Email'
Please select 'Agree to Terms'

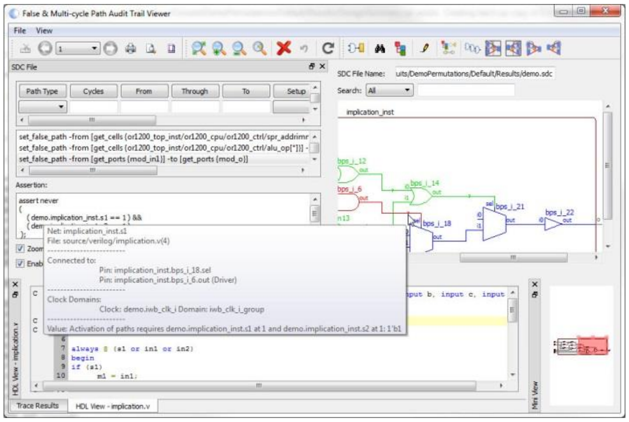
-

- Check IEEE Verilog/System Verilog & VHDL language specification compliance and syntax
- Configure checks along with standard checks, STARC, RMM, and AMD® UltraFast™ Design Methodology
- Use the GUI to streamline debug; integrated RTL, schematics, and message viewer
- Use easy debug message sorting, filtering and waiving to pinpoint problems
- Automated flow with Tcl-based Command Line Interface (CLI), and re-usable message waiver file

Identify Design Issues Quickly

The Visual Verification Suite's Analyze RTL enables users to debug design issues quickly using intelligent sorting and message filtering.

- Low Noise
- Check customization for specific design style
- Easy setup
- Waiver migration



False & Multi-cycle Path Audit Trail Viewer

SDC File Name: uits/DemoPermutations/Default/Results/demo.sdc

Search: All

Path Type	Cycles	From	Through	To	Setup

```
set_false_path -from [get_cells {or1200_top_inst/or1200_cpu/or1200_ctrl/spr_addrimr
set_false_path -from [get_cells {or1200_top_inst/or1200_cpu/or1200_ctrl/alu_op[*]}] -
set_false_path -from [get_ports {mod_in1}] -to [get_ports {mod_o}]
```

Assertion:

```
assert never
(
  ( demo.implication_inst.s1 == 1 ) &&
  ( dem
);
```

☑ Zoom
☑ Enab

Net: implication_inst.s1
File: source/verilog/implication.v(4)

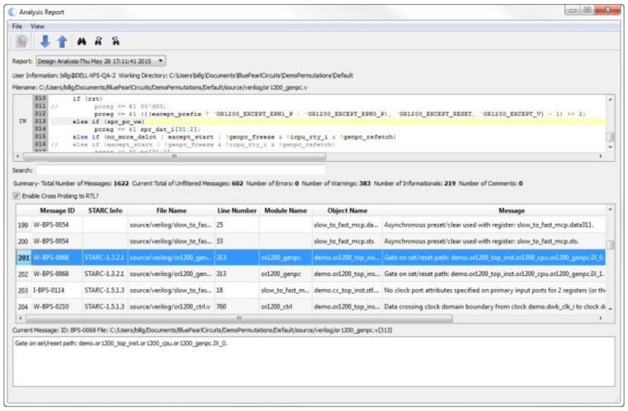
Connected to:
Pin: implication_inst.bps_i_18.sel
Pin: implication_inst.bps_i_6.out (Driver)

Clock Domains:
Clock: demo.iwb_clk_i Domain: iwb_clk_i_group

Value: Activation of paths requires demo.implication_inst.s1 at 1 and demo.implication_inst.s2 at 1: 1'b1

```
nput b, input c, input

always @ (s1 or in1 or in2)
begin
if (s1)
      m1 = in1;
```



Analysis Report

Report: Design Analysis-Thu May 28 17:11:41 2015

User Information: billg@DELL-XPS-QA-2 Working Directory: C:\Users\billg\Documents\BluePearlCircuits\DemoPermutations\Default

Filename: C:/Users/billg/Documents/BluePearlCircuits/DemoPermutations/Default/source/verilog/or1200_genpc.v

```
        if (rst)
//            pcreg <= #1 30'd63;
              pcreg <= #1 ({(except_prefix ? `OR1200_EXCEPT_EPH1_P : `OR1200_EXCEPT_EPH0_P), `OR1200_EXCEPT_RESET, `OR1200_EXCEPT_V} - 1) >> 2;
IW      else if (spr_pc_we)
              pcreg <= #1 spr_dat_i[31:2];
        else if (no_more_dslot | except_start | !genpc_freeze & !icpu_rty_i & !genpc_refetch)
//      else if (except_start | !genpc_freeze & !icpu_rty_i & !genpc_refetch)
```

Search:

Summary- Total Number of Messages: **1622** Current Total of Unfiltered Messages: **602** Number of Errors: **0** Number of Warnings: **383** Number of Informationals: **219** Number of Comments: **0**

☑ Enable Cross Probing to RTL?

	Message ID	STARC Info	File Name	Line Number	Module Name	Object Name	Message
199	W-BPS-0054		source/verilog/slow_to_fas...	25		slow_to_fast_mcp.da...	Asynchronous preset/clear used with register: slow_to_fast_mcp.data311.
200	W-BPS-0054		source/verilog/slow_to_fas...	33		slow_to_fast_mcp.sts	Asynchronous preset/clear used with register: slow_to_fast_mcp.sts.
201	W-BPS-0068	STARC-1.3.2.1	source/verilog/or1200_gen...	313	or1200_genpc	demo.or1200_top_ins...	Gate on set/reset path: demo.or1200_top_inst.or1200_cpu.or1200_genpc.IX_0.
202	W-BPS-0068	STARC-1.3.2.1	source/verilog/or1200_gen...	313	or1200_genpc	demo.or1200_top_ins...	Gate on set/reset path: demo.or1200_top_inst.or1200_cpu.or1200_genpc.IX_1.
203	I-BPS-0114	STARC-1.5.1.3	source/verilog/slow_to_fas...	18	slow_to_fast_m...	demo.cc_top_inst.stf...	No clock port attributes specified on primary input ports for 2 registers (or th
204	W-BPS-0210	STARC-1.5.1.3	source/verilog/or1200_ctrl.v	760	or1200_ctrl	demo.or1200_top_ins...	Data crossing clock domain boundary from clock demo.dwb_clk_i to clock d

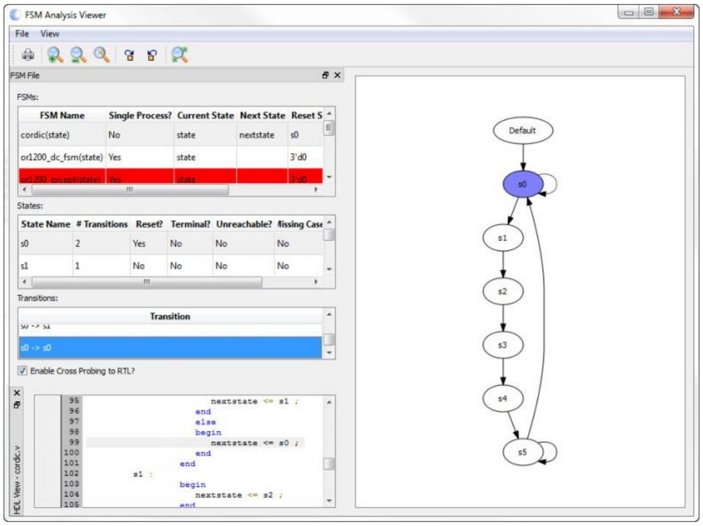
Current Message: ID: BPS-0068 File: C:/Users/billg/Documents/BluePearlCircuits/DemoPermutations/Default/source/verilog/or1200_genpc.v(313)

Gate on set/reset path: demo.or1200_top_inst.or1200_cpu.or1200_genpc.IX_0.

Finite State Machine Analysis

Rather than writing exhaustive simulation test benches to validate their finite state machines (FSMs), designers can use the FSM analysis capability within Analyze RTL. With minimal effort, designers can

- Extract FSMs from their RTL
- Find dead or unreachable states
- Generate easy to read bubble diagrams to better visualize FSMs



FSM Analysis Viewer

FSMs:

FSM Name	Single Process?	Current State	Next State	Reset S
cordic(state)	No	state	nextstate	s0
or1200_dc_fsm(state)	Yes	state		3'd0
or1200_except(state)	Yes	state		3'd0

States:

State Name	# Transitions	Reset?	Terminal?	Unreachable?	Missing Case
s0	2	Yes	No	No	No
s1	1	No	No	No	No

Transitions:

Transition
s0 -> s1
s0 -> s0

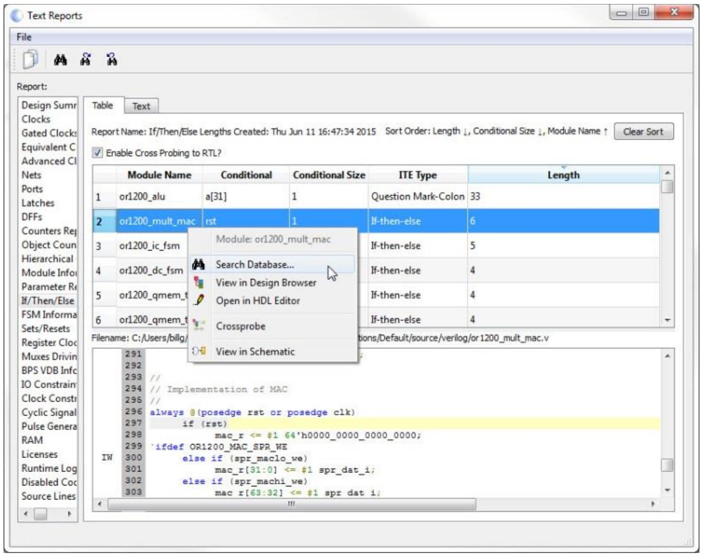
☑ Enable Cross Probing to RTL?

```
                    nextstate <= s1 ;
                 end
                 else
                 begin
                    nextstate <= s0 ;
                 end
              end
        s1 :
              begin
                 nextstate <= s2 ;
              end
```

RTL Checks for High Speed Designs

It is important to find as early as possible RTL coding that prevents the design from getting desired speed. FPGAs, because of their more constrained fabric than ASIC, certain type of structures causes slow down. Rather than wait for synthesis or static timing analysis results, Analyze RTL users can easily identify:

- High fanout nets
- Deep nested "if-then-else" statements
- High levels of logic paths
- Reset methodology, Async/sync



Text Reports

Report:

Report Name: If/Then/Else Lengths Created: Thu Jun 11 16:47:34 2015   Sort Order: Length ↓, Conditional Size ↓, Module Name ↑   Clear Sort

☑ Enable Cross Probing to RTL?

	Module Name	Conditional	Conditional Size	ITE Type	Length
1	or1200_alu	a[31]	1	Question Mark-Colon	33
2	or1200_mult_mac	rst	1	If-then-else	6
3	or1200_ic_fsm			If-then-else	5
4	or1200_dc_fsm			If-then-else	4
5	or1200_qmem_t			If-then-else	4
6	or1200_qmem_t			If-then-else	4

Filename: C:/Users/billg/ ... tions/Default/source/verilog/or1200_mult_mac.v

```
   //
   // Implementation of MAC
   //
   always @(posedge rst or posedge clk)
         if (rst)
               mac_r <= #1 64'h0000_0000_0000_0000;
   `ifdef OR1200_MAC_SPR_WE
IW       else if (spr_maclo_we)
               mac_r[31:0] <= #1 spr_dat_i;
         else if (spr_machi_we)
               mac_r[63:32] <= #1 spr_dat_i;
```