Blue Pearl Software

Accelerating Xilinx All Programmable FPGA and SoC Design Verification with Blue Pearl Software

Introduction

Xilinx All Programmable FPGAs and SoCs are used across multiple markets, powering applications such as machine learning, embedded vision, industrial IoT to cloud computing. With devices approaching 4,000K system logic cells, 12K DSP slices and multiple ARM cores, designs can be very complicated and swift verification may prove difficult with the vendor tools alone.

Typically, these systems are large, complex and partitioned into multiple clock domains and reset structures that are required to interface and control various subsystem. FPGA designers, developing these advanced SoCs, must not only develop functionally correct RTL, they must also ensure that the code is structurally correct to avoid simulation / hardware miss matches and metastability issues.

To reduce design risk and schedule slips, RTL code must be free of structural issues, adhere to industry and corporate coding best practices, be free of dead code and unreachable finite state machine (FSM) states, in addition to having synchronized clock domains crossings to avoid metastability. Failure to develop high reliability RTL can result in difficult and time consuming system level debug, as well as design iterations late in the design process when iteration times are at their longest.

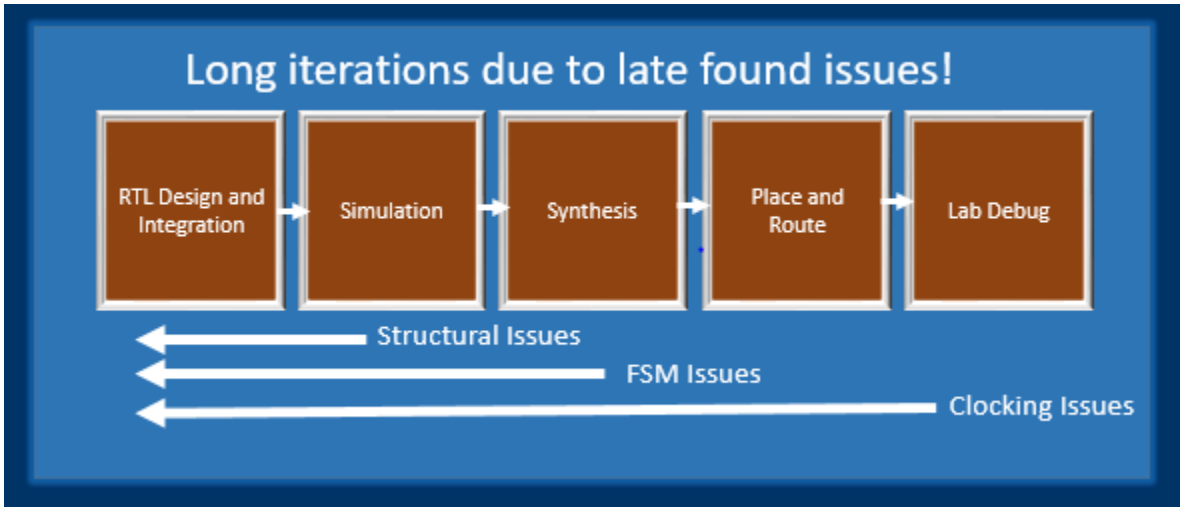
Blue Pearl Visual Verification Suite complements Xilinx® Vivado® Design Suite to accelerate verification with advanced structural and formal Linting and debug, Clock Domain Crossing Analysis and automatic SDC constraint generation. In addition, the Management Dashboard provides easy tracking as to the quality of the design based on required checks. It's ideal for reporting during design reviews and audits.

Now with the Blue Pearl Software Tcl App, available in the Xilinx Tcl Store, the Visual Verification Suite is tightly integrated into the Vivado graphical user interface. The app automates the task of loading synthesizable files from Vivado directly into the into the Visual Verification Suite. The app also enables the Visual Verification Suite's Management Dashboard to track progress over time not only in terms of the Visual Verification Suite's analysis results, but in terms of the timing, power, and utilization of Xilinx FPGA and SoC design as determined by Vivado.

Accelerating Verification While Improving QoR and Decreasing Risk

FPGA Vendor tools like Vivado Design Suite are designed to facilitate the transition from RTL code to final FPGA bit-stream as quickly and easily as possible. Debugging large design is very time consuming, however if you write bug-free RTL they work, very well.

Simulation is useful to find functional issues but it falls short when addressing structural issues. Many structural issues aren't found until synthesis, some not until implementation or worse yet, the lab, and others not at all. This results in long design iterations.

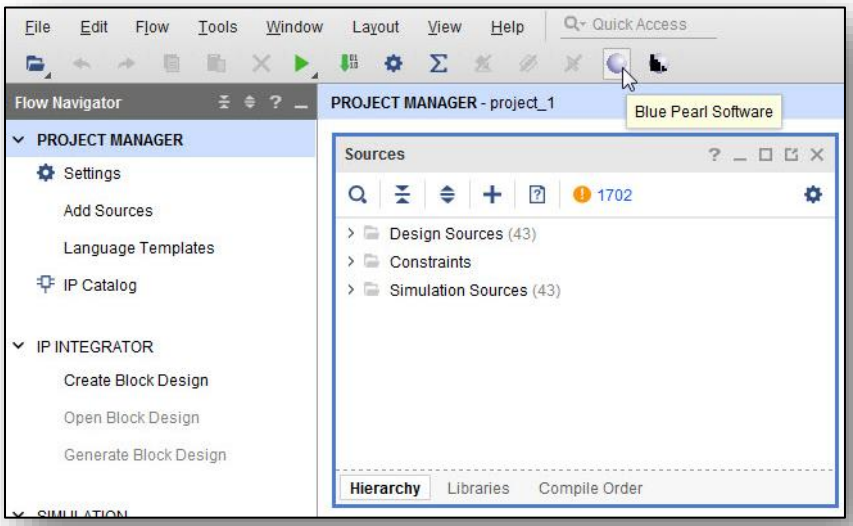


The Visual Verification Suite quickly finds and helps users understand and fix problems in their synthesizable HDL code, whether it's VHDL, Verilog, or SystemVerilog, by providing the industry's fastest find/fix rate for RTL bugs without the need to run simulation or synthesis. The Visual Verification suite eliminates time-consuming iterations through simulation and synthesis to increase productivity and enhance design reliability and re-usability by helping users write unambiguous HDL code that is correct-by-construction.

Accelerating FPGA & SoC Verification with the Visual Verification Suite

Leveraging the power of the Xilinx Tcl Store, Blue Pearl Software has created an app that lets you place Blue Pearl icons in the Vivado toolbar to launch the Visual Verification Suite with the current project opened and ready for analysis and debug. The app also collects and formats vital run-to-run information from your implementation results to be displayed by the Management Dashboard, such as Max Frequency, area, and power so that designers can quickly assess whether key design metrics are being improved or degraded over time.

Once the user has performed a one-time setup procedure, these two tasks require only one click each. Here's what it looks like:



With a click of a button, the design is loaded and the Visual Verification Suite of tools is setup, Xilinx libraries are loaded, and Xilinx UltraFast checks are enabled and ready for use. The tools provided with the Visual Verification Suite include:

- **Analyze RTL linting and debug** delivers comprehensive static RTL analysis to ensure error free, high QoR and quality designs. With Analyze RTL, users quickly find and fix design issues by leveraging industry standard and customer specific design rules, intelligent sorting, message filtering and block-to-top waiver migration.

- **Advanced clock and clock domain analysis** guarantees synchronized glitch free designs. It features graphical views of clocks and clock domain interactions, synchronized and unsynchronized crossing, along with User Grey Cell™ modeling for encrypted IP to ensure there are no missed CDC with encrypted IP.

- **Automatic SDC Generation** identifies false paths and multi cycle paths that constrain and slow downstream implementation tools and streamlines RTL simulation with automatic SVA or PSL assertions generation.

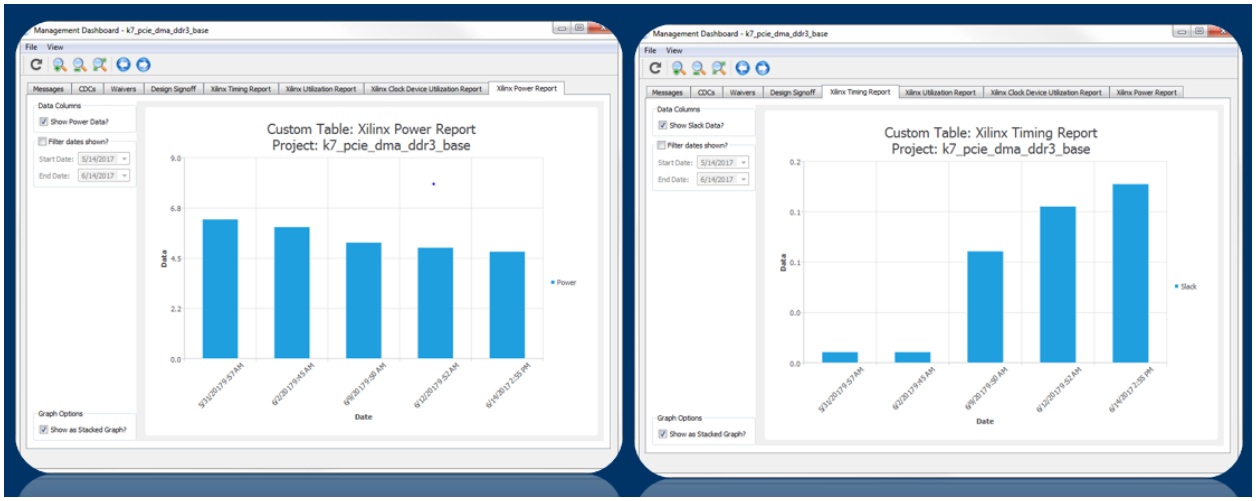
- **Management Dashboard** provides real-time visibility into RTL verification progress, run to run, providing graphical project reports that can be customized for documentation and design reviews. Reports highlight coverage, errors, warning and waivers for both Analyze RTL Linting and Clock Domain Crossing (CDC) solutions. The Design Sign-off ensures the code has been analyzed and has passed all user defined mandatory checks.

Tracking your design's progress with Management Dashboard

The Management Dashboard is built on top of the Visual Verification Suite's open standard SQL database. The tool monitors and logs messages, Clock Domain Crossings and waivers per run to provide real-time visibility into RTL verification progress.

Reports can be customized to omit or show errors, warnings, comments and info comments allowing managers and designers to quickly customize focused reports on areas of interest. The tool works for both interactive and batch runs making it useful for individuals as well as design teams working on multiple ASIC or FPGA system designs.

Now, using the Blue Pearl Tcl App, the Management Dashboard can be easily extended to gather key metrics from Vivado design runs as well. This can help users track key metrics such as FMax, Power, Area and more.



Graphs from the Management Dashboard are easily exported in Microsoft Office tools for inclusion into documentation and standard reports making it ideal for program updates and design reviews.

High Reliability RTL with a High ROI, While Improving QoR and Reliability

Advanced Linting, such as that provided by Blue Pearl has been customer proven to save approximately 4 weeks on a 16-week project. This equates to 25% shorter development cycle because issues are found as the user codes, and not later in the design cycle. In addition, approximately 1 in 4 designs will experience metastability issues which can take up to four weeks

to debug in the lab or 1 week for every 16 week project. This equates to a saving of 31%. The Visual Verification Suite not only provides high reliability it provides a high return on investment.

Blue Pearl Software App Details

The app has 3 public API calls, and is expected to be called via 2 GUI based add on buttons via the project based flow. At this time the App does not support non-project based flows.

The app was specifically designed to be as simple as possible and does not require parameters, using the current setup project.

The first flow, is to export a design that is setup in Vivado, into a Blue Pearl tcl project file using bpsvvs::generate_bps_project. The primary use of this, is a custom button to call the tcl command bpsvvs::launch_bps, which first calls generates_bps_project, then calls BluePearlVVE with the generated project as a parameter.

The second flow, is called after the user has implemented the design in Vivado, and calls the Visual Verification Suite with the project information as well as the utilization report, timing report and power report.

This information is used to extract the data and tracked by the customer over time to present in the Visual Verification Suite's Management Dashboard. This is done via the bpsvvs::update_vivado_into_bps command, and is also run from Vivado graphical interface add on button GUI button.

Conclusion

Blue Pearl's Visual Verification Suite is now tightly integrated with the Xilinx Vivado Design Suite so that designers can verify as the code and find and fix structural issues, metastability issues faster and more efficiently saving time and reducing risk. Download the app today from the Xilinx Tcl Store and contact your local Blue Pearl representative to try the Visual Verification Suite on your next design.

Further Reading

- Agile IP Development Process

  http://bluepearlsoftware.com/files/AgileIPDevelopment_Final.pdf

- RTL Analysis for Complex FPGA designs using a Grey Cell Methodology to Improve QoR
  http://www.bluepearlsoftware.com/files/GreyCell_WP.pdf

- Blue Pearl Tcl Reference Guide: *<installation>/doc/BluePearlTclReference.pdf*

- Blue Pearl Analyze Reference Manual: *<installation>/doc/BluePearlAnalyzeReference.pdf*

- Tcl online reference: http://www.tcl.tk
- PERL online reference: http://www.perl.com