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Xilinx's UltraFast Methodology: A Formula for Generation-Ahead Productivity

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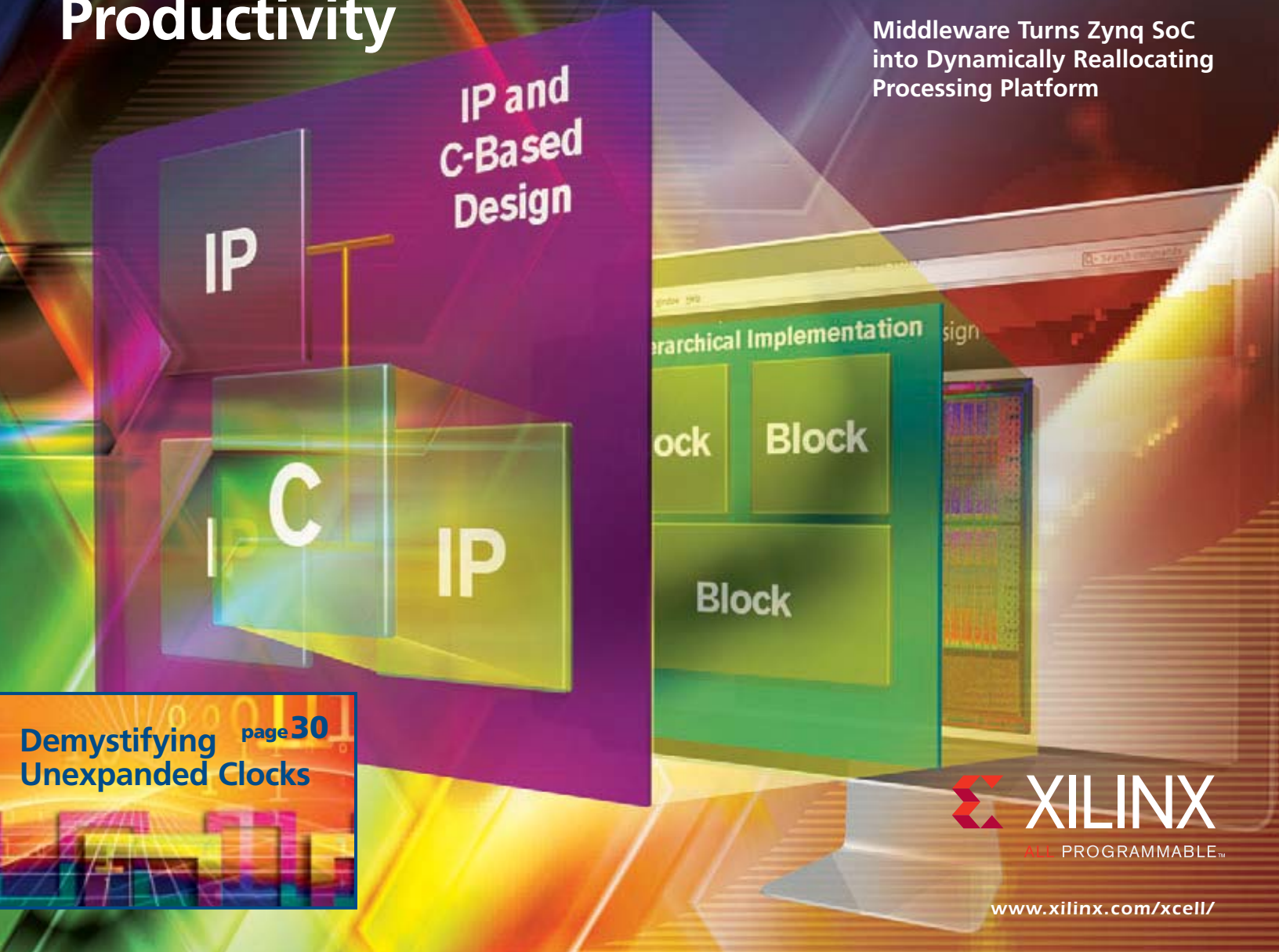

Demystifying Unexpanded Clocks page 30

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Xilinx's UltraFast Methodology: A Formula for Generation-Ahead Productivity

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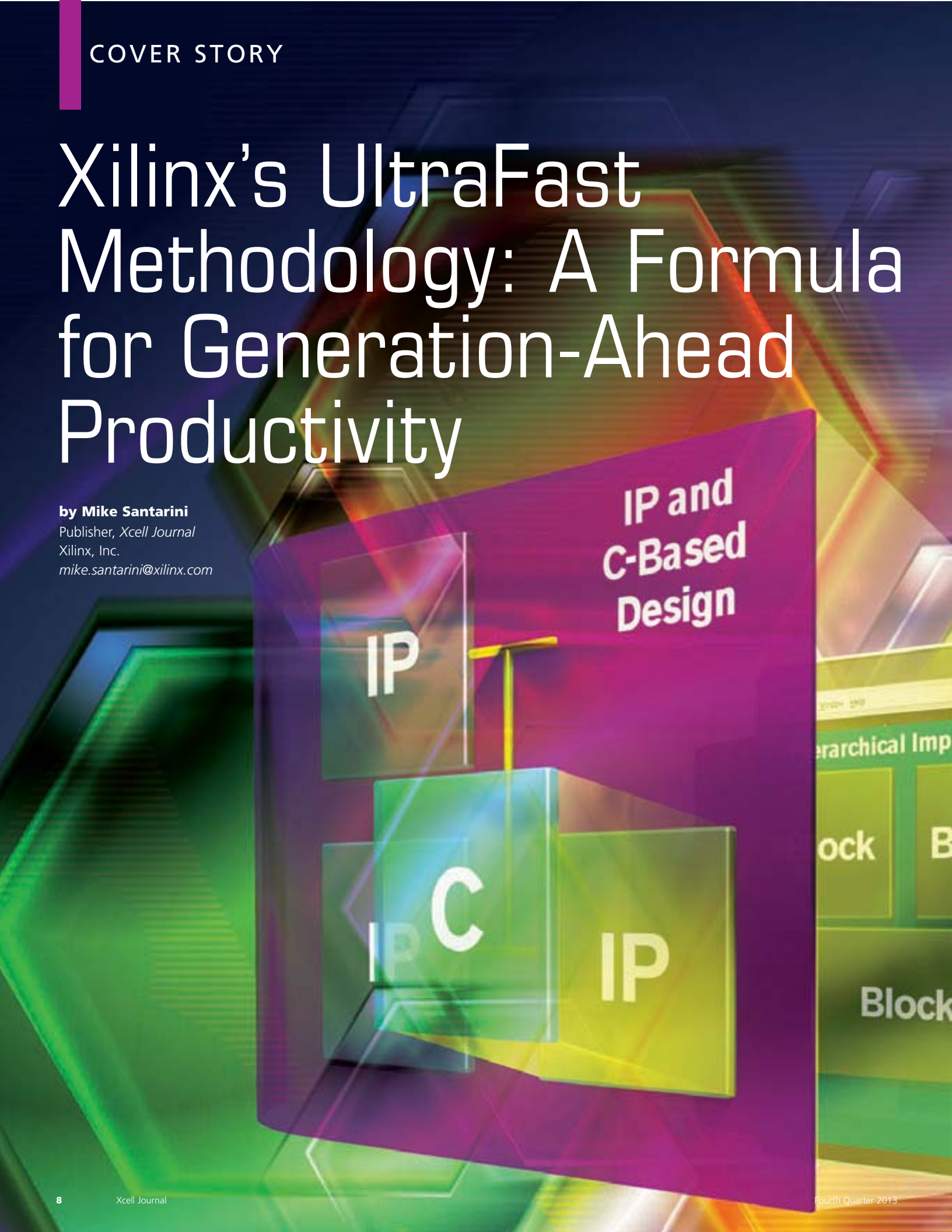

Hands-on techniques geared to tools in the Vivado Design Suite ensure predictable, repeatable results.

The relentless progression of IC process technology over the last 40 years has enabled electronics companies to create the boundless array of products we all enjoy today. But while this advancement of silicon process technology has been critically important to electronic innovation, it would not have been possible without the simultaneous and rapid evolution of tools from academia and the EDA industry. The progression from transistor-level SPICE simulation in the 1970s to today's highly advanced billion-gate system-level integrated design environments is truly remarkable. What's equally remarkable but often overlooked for its essential contribution to the electronics revolution is design methodology.

A design team can have access to the most advanced silicon in the world and the greatest tools in the world, but if the group doesn't establish a solid methodology it's difficult to deliver products at the right time and turn that rollout into business success. A good design methodology not only cuts down design time to allow teams to deliver quality products on deadline, but allows them to do so in a predictable and repeatable manner—a key to long-term business success. That said, methodologies must constantly evolve to take advantage of advances in both silicon and design tools.

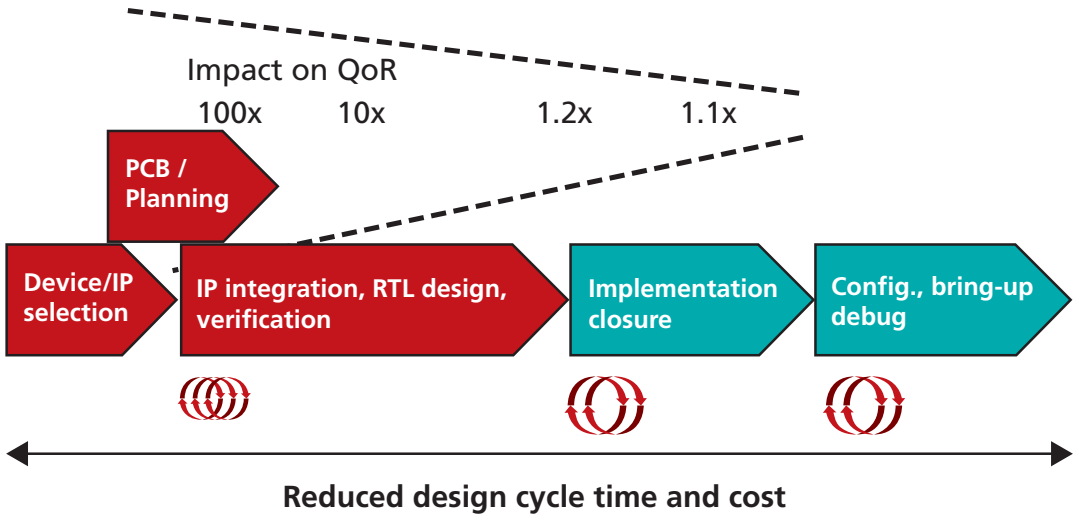

Figure 1 – Achieving closure at the beginning of the flow drastically improves the quality of results and cuts design time.

To help customers become even more productive and successful in rolling out next-generation innovations, Xilinx has just launched its UltraFast™ Design Methodology for design teams using the award-winning Vivado® Design Suite to implement designs in Xilinx®'s 28-nanometer 7 series and upcoming 20/16-nm UltraScale™ product families.

Ramine Roane, senior director of product marketing for the Vivado Design Suite, said this new methodology does not represent a radical shift; rather, with UltraFast, the company has hand-picked the best practices from industry experts and distilled these practices into a potent methodology that will speed design teams to predictable success. These best practices cover all aspects of board planning, design creation, design implementation and closure, programming and hardware debug.

"The UltraFast Design Methodology will enable design teams to take full advantage of the state-of-the-art technologies in the Vivado Design Suite and the Xilinx All Programmable devices, to accelerate productivity and repeatedly deliver designs to shorter, predictable schedules and thus deliver products to market sooner," said Roane.

The UltraFast methodology is yet another example of how Xilinx is maintaining its Generation Ahead lead over the competition. Xilinx not only has the best devices and most modern tool suite, but also the most comprehensive methodology in the industry.

To speed the adoption of the UtraFast Design Methodology, Xilinx has published a free methodology manual. *The UltraFast Methodology Guide for the Vivado Design Suite* (UG949) walks readers through an entire methodology, from board selection and RTL design to implementation and final debug. The document includes a comprehensive checklist designed to guide engineers throughout the design flow. Additionally, the 2013.3 release of the Vivado Design Suite automates many aspects of the methodology, including linting, and adds new DRC rule decks entitled "Methodology" and "Timing." The new version of the Vivado Design Suite also includes HDL and XDC templates, enabling an optimal-by-construction quality of results (QoR) for synthesis and implementation. Xilinx is also offering a series of free self-training videos online, as well as official training courses at various locations worldwide.

DESIGN METHODOLOGY FOR RAPID CONVERGENCE

Roane said that the UltraFast Methodology's main theme is to bring design closure to the front end of the design flow, where the impact on quality of results is greater (see Figure 1). And in this way, design teams can rapidly converge on a correct-by-construction design. "If you make informed decisions earlier in the flow levels, you will effectively eliminate much longer cycles in the implementation phases," said Roane.

Roane said this process was enabled by the Vivado Design Suite, which is the only design suite in the programmable industry to offer interactive design analysis and cross-probing to the sources at each step of the

flow, starting at design entry and continuing though IP integration, RTL synthesis, implementation (optimization, placement, physical optimization, routing) and bring-up. "With traditional tools, designers can only discover issues at the end of the process, on the fully implemented floorplan," said Roane. "If their design doesn't function as expected, their only choice is to backtrack to their initial design steps with little clue of what caused the problem, and incur many long iterative loops."

The key enabler of this cross probing and analysis capability is the Vivado Design Suite's unified data model. "The unified data model enables design teams to use the same analysis and closure routines throughout the entire flow," said Roane. "It's a huge advantage over older design suites, as it enables engineers to modify their design at multiple steps, even in-memory, and cross-probe any trouble area back to the sources or any other design view. Xilinx designed this unified data model to scale to high-end devices with many millions of logic cells, while competing tools have already started to break down on midrange devices."

Perhaps the best example to illustrate the UltraFast methodology's rapid design convergence is the concept of "baselining."

BASELINING TO RAPIDLY CONVERGE ON TIMING CLOSURE

"Baselining is a technique used to accelerate design convergence by focusing on internal F_{max}, which is the biggest problem nine times out of 10," said Roane. "This avoids wasting time with complex and extremely error-prone I/O constraints and timing exceptions, which can lead users and the tools in the wrong direction. With baselining, teams start the convergence process with the simplest of constraints, focused on flip-flop paths. Then—depending on whether the problem is in the clock path or a datapath, in an interconnect delay or logic delay—you apply the documented fixes and rerun the analysis."

Once design teams have closed timing with the baseline XDC, they're almost done. They then need to add I/O interface constraints. "It is important to ensure that these constraints are correct, in order to not create 'false' timing issues," said Roane. "This is why we provide XDC templates for source-synchronous, center-aligned DDR I/O constraints, for instance. If need be, constraints can be fine-tuned with timing exceptions or do a bit of floorplanning. But it is important to note that exceptions are not helpful, unless the corresponding paths show as critical. Similarly, over-floorplanning a design can be more harmful than helpful."

Roane said that baselining is not, however a substitute for sign-off constraints: "You still need to validate your design against complete constraints."

The UltraFast methodology also describes detailed steps to get to pristine sign-off constraints. Vivado automates this task with numerous batch and graphical routines to analyze timing paths, clock networks, interactions between clocks and more. The new Timing DRC rule deck can also be used for linting the constraints and clock networks in the design.

THE ULTRAFAST METHODOLOGY GUIDE FOR THE VIVADO DESIGN SUITE

To become familiar with the UltraFast Methodology, the first place to start is by

Baselining: A Technique for Rapid Design Closure

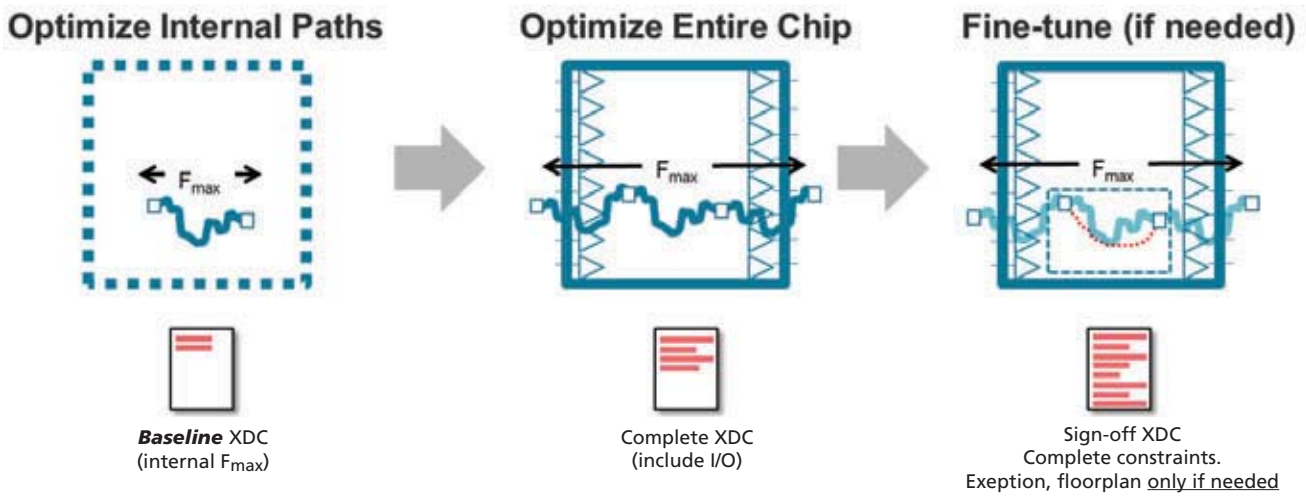

Figure 2 – Baselining allows design teams to quickly achieve timing closure.

reading *The UltraFast Methodology Guide for the Vivado Design Suite*. The guide is organized into six chapters, with the first two chapters introducing the content of the guide and recommendations for design suite flows. Chapters 3 through 6 dive deep into the best practices of the UltraFast methodology.

Chapter 3 addresses board and device planning and offers wise recommendations for PCB layout, clock resource planning and assignment, I/O planning design flows, FPGA power aspects and system dependencies. In order to avoid board respins, the methodology outlines the use of the Xilinx Power Estimator to explore and find architectures that meet the allocated power budget.

The chapter also emphasizes the importance of kicking off design projects with good I/O planning and recommends performing it in conjunction—or at least aligned—with board planning. Failing to align I/O and board planning can create timing and power distribution problems at a system level late in the process. The chapter also covers the various power modes, recommendations for power and thermal analysis, as well as cooling considerations for PCBs. It includes I/O recommendations when implementing Xilinx All Programmable 3D ICs in design projects, as the interposer connecting these multidice devices has unique requirements.

Chapter 4, "Design Creation," starts out with strategies and tips for creating a solid design hierarchy, selecting IP appropriate for your design, and then goes into several sections that offer practical RTL coding guidelines. It includes sections on control signals and sets, inferring RAM and ROM, coding for proper DSP and arithmetic inferences, coding shift registers and delay lines, and initialization of all inferred registers, SRLs and memories. The chapter includes a section on parameter attributes and constraints, as well as a section on clocking and whether to instantiate or infer.

'The way you write your HDL can make a big difference in how synthesis infers the logic. Good coding style will enable your design to use the hard blocks in the architecture and thus run at a higher frequency.'

"The way you write your HDL can make a big difference in how synthesis infers the logic," said Roane. "Good coding style will enable your design to use the hard blocks in the architecture and thus run at a higher frequency. To help customers leverage these resources to the fullest and thus speed their overall designs, we include templates to guide the inference of these components, particularly for RAM, shift registers and DSP resources. These templates are built into the Vivado Design Suite 2013.3"

Another highlight of the chapter are three sections dedicated to individual coding techniques for high reliability, improved performance and power optimization. Each section offers constraint recommendations to take advantage of the Vivado Design Suite's unified data model.

The section titled "Coding Styles for High Reliability" includes recommendations for clock domain crossings (synchronous and asynchronous), untimed resets and avoidance of combinatorial loops. The section on "Improved Performance" includes recommendations for high fan-outs in critical paths, register replication and considerations for implementing pipelining in designs. The "Coding Styles to Improve Power" section reviews various power-savings techniques you can employ in your design, from the tried-and-true datapath and clock gating to more subtle recommendations such as maximizing gating elements and keeping control sets in check.

Chapter 5 focuses on the implementation flow, from synthesis to routing. It kicks off with an overview of implementation, synthesis attributes and the advantages of a bottom-up flow. As discussed previously, the chapter includes a very deep look at timing analysis and introduces the concept of baselining for timing closure. Above and beyond that, the timing-closure section offers several great recommendations for what to do and what not to do for various timing problems you may encounter. It also covers considerations timing may have on power.

The last chapter in the guide, Chapter 6, covers configuration and debug. The first half walks readers through the best methods for generating a bitstream and programming the bitstream into your targeted Xilinx All Programmable device. The second half mainly presents best practices for debugging your design at multiple stages of the flow. This section discusses how to implement an HDL instantiation debug probing flow, or alternatively, how to use a netlist insertion debug probing flow. It also includes strategies for debugging the design once you've loaded it into your targeted device.

The guide's appendix provides a wealth of additional resources, perhaps the most significant being the UltraFast Design Methodology checklist, which highlights things a design team should consider at each stage in the cycle, from design planning to hardware debug. "It includes a lengthy list of questions highlighting the typical areas in which design decisions are likely to have downstream ramifications," Roane said. The checklist links readers to the areas in the guide or to external links that best describe that particular design concern. Xilinx also provides the checklist as a downloadable spreadsheet.

SUPPORT FOR THE ULTRAFAST METHODOLOGY

In addition to compiling all these best practices into the very useful *UltraFast Methodology Guide for the Vivado Design Suite*, Xilinx has incorporated many of the recommendations in the UltraFast methodology into its 2013.3 release of the Vivado Design Suite. With the 2013.3 release, the Vivado Design Suite now supports Methodology and Timing DRC rule decks to better guide users through design cycles, and includes very handy HDL and constraints templates for correct-by-construction designs.

In addition, Xilinx's worldwide training staff and Alliance Member ecosystem are actively supporting the UltraFast methodology.

For example, Blue Pearl Software has added Xilinx UltraFast design rules to its Analyze RTL linting tool. "Blue Pearl automates the RTL guidelines outlined in the UltraFast methodology," said Roane. "In addition to performing language linting, it enforces coding styles that give the optimal QoR for Xilinx devices, such as use of the right type of reset, or coding a RAM or a MAC in a way to infer our built-in blocks in the most optimal way."

In addition to third-party EDA support, Xilinx has been actively testing its IP to ensure it conforms to the UltraFast methodology and DRCs and is actively encouraging Alliance Member IP vendors to ensure they comply to these same guidelines as well.

Last but not least, the company is launching a series of training classes conducted by Xilinx and partners worldwide. It is also releasing a new UltraFast methodology QuickTake video. In addition, all new Xilinx videos will also incorporate the UltraFast guidelines.

To download a PDF version of the *UltraFast Design Methodology Guide* for the Vivado Design Suite (UG949) and for further information on the UltraFast Methodology, visit *www.xilinx.com/ultrafast*.