Blue Pearl Software Speeds Up FPGA Verification with Release 7.2

Extends support for multi-cycle paths and user-specified design constraints checking

Santa Clara, California – December 06, 2013 -- Blue Pearl Software, the provider of EDA software that accelerates FPGA verification, today announced that it is shipping Release 7.2 of its software, Blue Pearl Software Suite, for Windows® and Linux® operating systems. It includes design constraints checking and multi-cycle path (MCP) enhancements including finite state machine (FSM) and sequential analysis.

"Release 7.2 automates the generation of Synopsys design constraints (SDC) for complex non-cyclical MCPs," said Ellis Smith, Chairman and CEO, Blue Pearl Software. "Additionally, the SDC verification feature will improve the accuracy and quality of SDC constraints while significantly reducing tedious manual reviews."

Designers are faced with the difficult task of meeting all the design requirements, e.g. lower power consumption with increasing functional speed and feature set. Thus, designers resort to constraints, typically in SDC format, to accelerate implementation. It is relatively straightforward to write structural design constraints for port and clocks but this is an error prone task. The SDC constraint verification capability in release 7.2 validates user-specified SDC constraints. It flags issues such as incorrectly generated clock definitions, port delay constraints and IO ports constraints. SDC Verification ensures correctness and consistency of constraints by pinpointing the root cause of constraint problems, thus trimming weeks from design schedules.

Additional Release 7.2 new features include methodology-specific messaging for Xilinx and STARC, improved false path, clock domain crossing and MCP analysis through bidirectional ports, improved FSM-based MCP analysis, and support for MCP sequential analysis.

Price and Availability

Release 7.2 of the Blue Pearl Software Suite is available now. The base product, RTL analysis, starts at $10K for a floating 1-YR TBL, with the other options CDC and SDC priced at $10K,

and $15K respectively. Please contact sales@bluepearlsoftware.com to arrange a demo, or for additional pricing and upgrade information.

The Blue Pearl Software Suite is also available for online purchase via the Embedded Software Store or the Blue Pearl Software online store. For more information about the online stores, please visit http://embeddedsoftwarestore.com/store or https://store.bluepearlsoftware.com/1112/catalog/catalog.1018/.

For more information about Blue Pearl Software, please visit www.bluepearlsoftware.com.

About Blue Pearl Software

Blue Pearl Software, Inc. provides EDA software that accelerates FPGA design verification. The company's Blue Pearl Software Suite checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA design risks.

Visit Blue Pearl Software at http://www.bluepearlsoftware.com.

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