Blue Pearl Joins Xilinx Alliance Program, Accelerates Design Implementation

Blue Pearl's Efficient SDC Generation, Improves All Programmable Design Timing

SANTA CLARA, California–May 29, 2012 -Blue Pearl Software, Inc., a leading provider of EDA software that accelerates field-programmable gate array (FPGA) implementation, announced that it has joined the Xilinx Alliance Program. Xilinx Inc. is the worldwide leader and developer of *All Programmable* devices. As a result of its Xilinx collaboration, Blue Pearl announces improved productivity for Xilinx Vivado™ Design Suite users, by reducing development time, run time and the number of design iterations.

Blue Pearl Software Suite accelerates the process of identifying timing-critical paths. It works with the recently announced Xilinx Vivado Design Suite and automatically generates SDCs that result in more efficient synthesis runs and enables timing-driven place and route.

The Xilinx Alliance Program includes companies that provide new design methodologies and IP cores to quickly meet customers' performance, power and cost targets. The program is comprised of leading companies across the world, that are trained to take full advantage of the features in Xilinx Platform FPGAs, Zynq Extensible Processing Platform, tools and IP cores.

"We have been working for more than six months with Xilinx to support their products and their new Vivado Design Suite," said Shakeel Jeeawoody, VP Marketing at Blue Pearl Software. We confirmed that the Blue Pearl Software Suite makes synthesis more efficient, accelerates implementation and improves timing for users of the Xilinx flow."

"We are pleased to strengthen our connection with Blue Pearl and welcome them as a new member of our Xilinx Alliance Program member," said Tom Feist, Senior Director of Design Methodology Marketing at Xilinx. "Xilinx has taken advantage of industry standards when developing the Vivado Design Suite to improve ease of use and expand our customer's ability to leverage solutions like those provided by Blue Pearl to improve productivity accelerating their time-to-market and ability to gain a competitive advantage."

To read more about how Blue Pearl Software takes the pain out of FPGA synthesis, please click here.

About Blue Pearl Software Suite
Blue Pearl Software Suite accelerates FPGA implementation with comprehensive RTL analysis, CDC checks and automatic SDC generation. Its Visualization Verification Environment ™ and design technology give users immediate feedback for validating automatically generated pre-synthesis longest paths and SDCs, which are s used to drive the efficiency of synthesis and place & route tools.

About Xilinx Vivado Design Suite
The Xilinx Vivado Design Suite is a revolutionary IP and system-centric design environment built from the ground up to accelerate the design of not only programmable logic and I/O but 'All Programmable' devices. The Vivado Design Suite is already proven to accelerate integration and implementation by up to 4x over traditional design flows, reducing cost by simplifying design and automating – not dictating – a flexible design environment.

About Xilinx Alliance Program
The Xilinx Alliance Program is a worldwide ecosystem of qualified companies collaborating with Xilinx to help customers develop products faster and with confidence on Targeted Design Platforms. Leveraging open platforms and standards, Xilinx has built this ecosystem to meet customer needs and is committed to its long-term success. Comprised of FPGA IP providers, EDA vendors, embedded software providers, system integrators, and hardware suppliers, Alliance members help accelerate the design process while minimizing risk.

About Xilinx
Xilinx develops All Programmable technologies and devices, beyond hardware to software, digital to analog, and single to multiple die in 3D ICs. These industry leading devices are coupled with a next-generation design environment and IP to serve a broad range of customer needs, from programmable logic to programmable systems integration. For more information, visit http://www.xilinx.com/.

About Blue Pearl Software
Blue Pearl Software, Inc. provides next generation EDA software that uses new and innovative technology to reduce design flow iterations and increase designer productivity early in the digital design flow. Blue Pearl Software Suite checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA and ASIC design risks.
Visit Blue Pearl Software at http://www.bluepearlsoftware.com.

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Acronyms
ASIC: Application Specific Integrated Circuit
CDC: Clock Domain Crossing
EDA: Electronic Design Automation
FPGA: Field Programmable Gate Array
RTL: Register Transfer Level
SDC: Synopsis Design Constraints