Blue Pearl Announces Release 6.0 of EDA Software Suite with SystemVerilog and FPGA Enhancements

Demos at DVCon, Feb. 28-29, 2012, Doubletree Hotel, San Jose, California

SAN JOSE, Calif. -February 16, 2012 -Blue Pearl Software, Inc, the provider of next generation EDA software that increases designer productivity and design quality, announced that it is shipping Release 6.0 of its EDA software, **Blue Pearl Software Suite**, for Windows and Linux operating systems. It includes enhancements that improve support for SystemVerilog and VHDL, as well as FPGA design.

"Our 6.0 Release improves support for SystemVerilog and VHDL and the FPGA synthesis flow," said Shakeel Jeeawoody, Director of Product Marketing at Blue Pearl. "Designers can now mix and match hardware languages in the same design, with language checking that matches their downstream tools."

Blue Pearl Software Suite offers comprehensive RTL analysis, clock-domain crossing (CDC) checks, and automatic Synopsys Design Constraints (SDC) generation for FPGA, ASIC and SOC designs. Its visualization and validation technology gives users immediate feedback for validating automatically generated timing constraints.

Release 6.0 features include:

Multi-language support	*We have added full language support for SystemVerilog and VHDL, so now designers can mix/match any combination of Verilog, SystemVerilog and VHDL in the same design.*
Longest Path Viewer	*Users can now visualize the longest paths of their design using the new longest path viewer.*
Improved FPGA synthesis flow	*The improved flow with Synplify Pro enables better handling of SDC constraints*
Improved support for Finite State Machine issues	*Improved detection of unreachable states.*
Improved waiver handling	*User can now select multiple messages at once to apply waivers*
Improved message viewing in Analysis Report viewer	*The text of the currently selected message is displayed in full below the overall report.*
Easier to setup/verify DFT checks	*You can now specify initialization patterns, scan chains, and test procedures from the GUI.*
Stricter language checks	*The tool now does stricter language checks to match downstream products in the flow.*
Improved support for -f files	*Users can now both specify a .f file and use the GUI to specify additional input files.*

To Learn More

Blue Pearl Software Suite will be demonstrated at the Design and Verification Conference (DVCon), Feb. 28-29, in Booth #405, DoubleTree Hotel, San Jose, California.

FPGA designers can learn more by registering at http://www.bluepearlsoftware.com/fpga/.

Blue Pearl also offers hands-on workshops and software evaluations.

Price and Availability

Release 6.0 of Blue Pearl Software Suite is available now. Please contact sales@bluepearlsoftware.com to arrange a demo, or for pricing and upgrade information.

About Blue Pearl Software

Blue Pearl Software, Inc. provides next generation EDA software that uses new and innovative technology to reduce design flow iterations and increase designer productivity early in the digital design flow. Blue Pearl Software Suite checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA and ASIC design risks.

Visit Blue Pearl Software at http://www.bluepearlsoftware.com.

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Acronyms

ASIC:	Application Specific Integrated Circuit
CDC:	Clock Domain Crossing
EDA:	Electronic Design Automation
FPGA:	Field Programmable Gate Array
RTL:	Register Transfer Level
SDC:	Synopsis Design Constraints
SOC:	System on Chip

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