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Blue Pearl Software Announces Support for Synopsys Synplify Pro Design Flow

See Blue Pearl at DATE March 13-15, 2012, Dresden, Germany;
Demos at SNUG, March 26, 2012, Santa Clara, California

SANTA CLARA, California, USA. and **DRESDEN**, Germany –13 March 2012 -Blue Pearl Software, Inc, a provider of next generation EDA software that increases designer productivity and design quality, announced that its **Blue Pearl Software Suite**, for Windows and Linux operating systems, supports Synopsys' Synplify Pro® FPGA synthesis software for VHDL and SystemVerilog designs.

Blue Pearl Software will be at Design, Automation, and Test in Europe (DATE) conference in Dresden, Germany, March 13-15, 2012, booth #3 and at Synopsys User Group (SNUG) Designer Community Expo, Santa Clara Convention Center, Santa Clara, California, March 26, 2012, open to all registered attendees of SNUG Silicon Valley.

Blue Pearl Software Suite's connection to Synplify Pro software improves interoperability with Synopsys' leading synthesis flow and makes it easier for FPGA designers to add Blue Pearl Software's automatic Synopsys Design Constraints (SDC) generation to their flow. It offers users improved constraint analysis and a solution that minimizes design risks.

"Our collaboration with Synopsys resulted in an optimized flow that works with Synplify Pro FPGA synthesis software," said Shakeel Jeeawoody, director of product marketing at Blue Pearl. "VHDL and SystemVerilog designers are now able to automatically generate an exhaustive set of constraints that address false and multi-cycle paths and that work with Synopsys' leading synthesis flow."

Blue Pearl Software Suite offers comprehensive RTL analysis, clock-domain crossing (CDC) checks, and automatic Synopsys Design Constraints (SDC) generation for FPGA, ASIC and SOC designs. Its visualization and validation technology gives users immediate feedback for validating automatically generated pre-synthesis longest paths and SDC timing constraints.

Last month, Blue Pearl Software announced Release 6.0 of its Blue Pearl Software Suite with capabilities that support FPGA designers.

To Learn More

FPGA designers can learn more by visiting http://www.bluepearlsoftware.com/fpga/ , signing up for a hands-on workshops or software evaluation.

Price and Availability

The Blue Pearl Software Suite for FPGA design with Synplify Pro is available now. Please contact sales@bluepearlsoftware.com to arrange a demo, or for pricing and upgrade information.

About Blue Pearl Software

Blue Pearl Software, Inc. provides next generation EDA software that uses new and innovative technology to reduce design flow iterations and increase designer productivity early in the digital design flow. Blue Pearl Software Suite checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA and ASIC design risks.

Visit Blue Pearl Software at http://www.bluepearlsoftware.com.

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Acronyms

ASIC:	Application Specific Integrated Circuit
CDC:	Clock Domain Crossing
EDA:	Electronic Design Automation
FPGA:	Field Programmable Gate Array
RTL:	Register Transfer Level
SDC:	Synopsis Design Constraints
SOC:	System on Chip