At the 49th Design Automation Conference, Blue Pearl Showcases Interoperability with Leading FPGA Ecosystem Players, Focuses on Accelerating FPGA Implementation & IP Subsystem Integration

Who/What

At the Design Automation Conference (DAC), Blue Pearl Software, a leading provider of EDA software that accelerates field-programmable gate array (FPGA) implementation, will showcase its Blue Pearl Software Suite's interoperability with tools and flows from other leading FPGA ecosystems players- Xilinx Vivado™ Design Suite and Synopsys Synplify Pro™ FPGA synthesis software.

The Blue Pearl Software Suite provides Register Transfer Level (RTL) analysis includes linting, clock domain crossing (CDC) and automatic Synopsys Design Constraint (SDC) generation and makes the synthesis and place and route phases of FPGA design implementation more efficient. Its Visual Verification Environment™ makes it easy to use for any level of designer.

With the Blue Pearl Software Suite, Verilog, VHDL and SystemVerilog designers using Windows or Linux, can automatically generate an exhaustive set of constraints that address false and multi-cycle paths, accelerate their embedded system development and improve design quality (QoR) because of Blue Pearl's collaboration with the world's leading FPGA tool suppliers and intellectual property (IP) providers.

When/Where

Monday-Wednesday, June 4-6, from 9 am to 6 pm
Booth #714
Moscone Convention Center, San Francisco, California

For More Information

To schedule a meeting with Blue Pearl, please click here.
For more information, please visit Blue Pearl Software at http://www.bluepearlsoftware.com.
For more information about DAC, please visit www.dac.com

About Blue Pearl Software

Blue Pearl Software, Inc. provides next generation EDA software that uses new and innovative technology to reduce design flow iterations and increase designer productivity early in the digital design flow. Blue Pearl Software Suite checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA and ASIC design risks.
Visit Blue Pearl Software at http://www.bluepearlsoftware.com.

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Acronyms

ASIC:	Application Specific Integrated Circuit
CDC:	Clock Domain Crossing
EDA:	Electronic Design Automation
IP:	Intellectual Property
QoR:	Quality of Results
RTL:	Register Transfer Level
SDC:	Synopsys Design Constraints