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Blue Pearl Announces North American Expansion

Supports Growing Market in FPGA Design Software

SANTA CLARA, CA--(Marketwire - Dec 18, 2012) -- Blue Pearl Software, the provider of EDA software that accelerates RTL signoff for FPGA designs, today announced it has added sales and support staff in North America due to the increased interest in using the Blue Pearl Software Suite for designs in the embedded, military and medical devices markets.

The new North American Director, Western Region sales is Dave Burton, and the Director, Eastern Region sales is Walt Brennan. They have extensive sales experience with leading EDA companies.

"By adding experienced sales and support staff to our teams on the eastern and western region of the United States, we are providing support to our growing customers who are designing complex FPGAs" remarked Ellis Smith, Blue Pearl Software CEO.

To contact Blue Pearl Software's sales and support offices, please visit
http://www.bluepearlsoftware.com/company/contact/

About the Blue Pearl Software Suite for FPGA RTL Signoff
The Blue Pearl Software Suite works with the Xilinx Vivado Design Suite running on Windows platforms. It includes linting, CDC analysis and automatic SDC generation. Its generated SDCs drive the efficiency of the synthesis and place and route phases of FPGA design implementation, and reduce iterations and overall design time. Its Visual Verification Environment™ makes it easy to use.

The company's collaboration with Synopsys offers an optimized flow that works with Synopsys' Synplify Pro FPGA synthesis software. Verilog, VHDL and SystemVerilog designers can automatically generate an exhaustive set of constraints that address false and multi-cycle paths that are compatible with Synopsys' synthesis flow.

About Blue Pearl Software
Blue Pearl Software, Inc. provides EDA software that accelerates RTL signoff for FPGA designs to improve quality of results (QoR) and reduce FPGA design risks. The Blue Pearl Software Suite finds and analyzes the longest path using the RTL design (rather than the netlist), generates SDCs automatically for false and multi-cycle paths, enables full-chip CDC analysis by improving inter-IP analysis using its Grey Cell methodology, and determines the number of logic levels in a design to analyze resource usage for best fit into the target FPGA.

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Acronyms

CDC: Clock Domain Crossing
EDA: Electronic Design Automation
FPGA: Field Programmable Gate Array
QoR: Quality of Results
RTL: Register Transfer Level
SDC: Synopsys Design Constraints
SoC: System-on-Chip

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