

At SAME 2012, Blue Pearl Software & ADACSYS Present on Best FPGA Electronic Design Practices and Demonstrate Solutions

Sophia Antipolis, France

Who/What

At the Sophia Antipolis MicroElectronics forum ([SAME](#) 2012), [Blue Pearl Software](#), a leading provider of EDA software that accelerates field-programmable gate array (FPGA) implementation, and [ADACSYS](#), a provider of functional verification and test software for accelerated verification of FPGA Intellectual Property (IP) blocks and designs, are presenting a tutorial on *Best FPGA Design Practices*. During [SAME](#), the companies will be demonstrating solutions at the ADACYS Stand # 20.

When/Where

Session 3: [Advanced Design Methodologies](#)

Tutorial: *Best FPGA Design Practices*

13h30-15H00, Wednesday, 3 October, 2012

Demos: ADACSYS Stand # 20

CICA

2229 Route des Crêtes

06560 Sophia Antipolis-France

<http://www.cica.fr/fr/plans/index.html>

For More Information

To schedule a meeting with Blue Pearl, please email sales@bluepearlsoftware.com.

For more information, please visit <http://www.bluepearlsoftware.com>.

For more information about SAME 2012, please visit <http://www.same-conference.org/>.

About ADACSYS

[ADACSYS](#) is a start-up specializing in FPGA-based High Performance Computing (HPC) solutions. ADACSYS provides tools to accelerate the physical tests and debug of embedded applications for aeronautics, FPGA designs and ASIC FPGA-based prototyping markets. <http://www.adacsys.com>

About Blue Pearl Software

[Blue Pearl Software, Inc.](#) provides next generation EDA software that uses new and innovative technology to reduce design flow iterations and increase designer productivity early in the digital design flow. [Blue Pearl Software Suite](#) checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA and ASIC design risks. <http://www.bluepearlsoftware.com>

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