Blue Pearl Advances FPGA Design Automation, Announces Software Release with Enhanced Path Analysis

Demos set for ARM TechCon, Oct.31-Nov 1, 2012, Santa Clara, California

SAN JOSE, Calif. -October 19, 2012 -Blue Pearl Software, Inc., the provider of EDA software that accelerates RTL signoff for FPGA designs, today, announced that it is shipping Release 6.1 of its **Blue Pearl Software Suite**, for Windows and Linux operating systems. The new version includes enhancements that improve and further automate the FPGA design process, including one of its biggest design bottlenecks - critical path analysis.

"Our goal is to alleviate painful parts of the FPGA design process coupled with easy to use EDA software," remarked Shakeel Jeeawoody, VP Marketing at Blue Pearl. "With the 6.1 release, FPGA designers have more control over tool flow and mode-based path analysis before running synthesis and timing analysis."

What's New in 6.1

Enhancements to Blue Pearl Software Suite Version 6.1 include:

- Mode-based path analysis
- Better tool control using TCL
- Enhanced CDC schematics to pinpoint problems

Previously announced, 6.0 enhancements included multi-language (SystemVerilog, VHDL, and Verilog) support, a longest path viewer and an improved FPGA synthesis flow.
For more information, on longest path analysis, please click here to read our article *Find and Analyze the Longest Combinational Paths, Meet Performance Goals*.

About the Blue Pearl Software Suite for FPGA RTL Signoff

The Blue Pearl Software Suite works with the Xilinx Vivado Design Suite running on Windows platforms. It includes linting, CDC analysis and automatic SDC generation. Its generated SDCs automate the synthesis and place and route phases of FPGA design implementation, and reduce iterations and overall design time. Its Visual Verification Environment™ makes it easy to use.

The company's collaboration with Synopsys offers an optimized flow that works with Synopsys'

Synplify Pro FPGA synthesis software. Verilog, VHDL and SystemVerilog designers can automatically generate an exhaustive set of constraints that address false and multi-cycle paths that are compatible with Synopsys' synthesis flow.

To Learn More

Blue Pearl Software Suite will be demonstrated at ARM TechCon 2012, Oct. 31-Nov. 1, stand TT2, Santa Clara Convention Center, Santa Clara, California.

Please click on the following links to sign up for a hands-on workshops and software evaluations.

Price and Availability

Release 6.1 of Blue Pearl Software Suite is available now. Please contact sales@bluepearlsoftware.com to arrange a demo or for pricing and upgrade information.

About Blue Pearl Software

Blue Pearl Software, Inc. provides EDA software that accelerates RTL signoff for FPGA designs. The company's Blue Pearl Software Suite checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA design risks.

Visit Blue Pearl Software at http://www.bluepearlsoftware.com.

###

Press Contact:
Georgia Marszalek, ValleyPR, LLC for Blue Pearl Software, +1-650.345.7477, Georgia@ValleyPR.com

Notes to editors
A Blue Pearl Software Suite 6.1 graphic is available on request.

Acronyms

ASIC:	Application Specific Integrated Circuit
CDC:	Clock Domain Crossing
EDA:	Electronic Design Automation
FPGA:	Field Programmable Gate Array
RTL:	Register Transfer Level
SDC:	Synopsys Design Constraints
SOC:	System on Chip
Tcl:	Tool Command Language