

Blue Pearl Software announces new distributor for Taiwan

SAN JOSE, Calif.(Business Wire) -April 18, 2013 - Blue Pearl Software, Inc, the provider of RTL Signoff EDA software for FPGAs, announced the appointment of Kaviatz Technology Co., Ltd as its distributor in Taiwan. The Kaviatz team will provide sales and technical support of the popular Blue Pearl Software Suite in Taiwan.

“Blue Pearl Software is excited to partner with Kaviatz Technology – they are a recognized leader in Taiwan for their technical skills and technical relationship management, said Roger Bitter, Vice President Worldwide Sales, Blue Pearl Software. Our customers will benefit from Kaviatz’s strong values to pursue the spirit of service”

The Blue Pearl Software Suite works with the Xilinx Vivado Design Suite running on Windows platforms. It includes linting, CDC analysis and automatic SDC generation. Its generated SDCs drive the efficiency of the synthesis and place and route phases of FPGA design implementation, and reduce iterations and overall design time. Its Visual Verification Environment™ makes it easy to use.

The company’s collaboration with Synopsys offers an optimized flow that works with Synopsys’ Synplify Pro FPGA synthesis software. Verilog, VHDL and SystemVerilog designers can automatically generate an exhaustive set of constraints that address false and multi-cycle paths that are compatible with Synopsys’ synthesis flow.

For information, on Blue Pearl’s [longest path analysis](#), please [click here](#) to read our article [Find and Analyze the Longest Combinational Paths, Meet Performance Goals](#).

For information on how Blue Pearl enables SoC RTL analysis, [click here](#) to read our white paper, [RTL analysis for complex FPGA designs using a Grey Cell methodology](#).

About Kaviatz Technology

Kaviatz Technology Co., Ltd was established during 2008 for the purpose of providing the best support possible to high tech companies in Taiwan. With our dedicated support, we are successful in representing many EDA and IP companies in Taiwan.

Visit Kaviatz at www.kaviatztech.com

About Blue Pearl Software

Blue Pearl Software, Inc. provides RTL Signoff software that uses new and innovative technology to reduce design flow iterations and increase designer productivity early in the digital design flow. By partnering with key players of the FPGA Ecosystem, Blue Pearl Software accelerates FPGA implementation. Blue Pearl Software Suite checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDC) to improve quality of results (QoR) and reduce FPGA and ASIC design risks.

Visit Blue Pearl Software at <http://www.bluepearlsoftware.com>.

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Press Contact:

Shakeel Jeeawoody, Blue Pearl Software, +1- 408.961.0121, shakeel@bluepearlsoftware.com

Acronyms

ASIC: Application Specific Integrated Circuit
CDC: Clock Domain Crossing
EDA: Electronic Design Automation
FPGA: Field Programmable Gate Array
RTL: Register Transfer Level
SDC: Synopsys Design Constraints
SOC: System on Chip
Tcl: Tool Command Language

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