

## Blue Pearl Demos FPGA Design Tools for RTL Signoff, Improves QoR at ARM TechCon

### Who

[Blue Pearl Software](#), the provider of EDA software that accelerates RTL signoff for FPGA designs

### What

Demonstrations of the [newest version](#) of the [Blue Pearl Software Suite](#) at [ARM TechCon](#)

### When/Where

Oct. 31-Nov. 1, 2012, stand TT2  
Santa Clara Convention Center  
Santa Clara, California

### About the Blue Pearl Software Suite for FPGA RTL Signoff

The [Blue Pearl Software Suite](#) works with the Xilinx Vivado Design Suite running on Windows platforms. It includes linting, CDC analysis and automatic SDC generation. Its generated SDCs automate the synthesis and place and route phases of FPGA design implementation, and reduce iterations and overall design time. Its Visual Verification Environment™ makes it easy to use.

The company's collaboration with Synopsys offers an optimized flow that works with Synopsys' Synplify Pro FPGA synthesis software. Verilog, VHDL and SystemVerilog designers can automatically generate an exhaustive set of constraints that address false and multi-cycle paths that are compatible with Synopsys' synthesis flow.

### To Learn More

Please click on the following links to sign up for a [hands-on workshops](#) and [software evaluations](#).

For information, on Blue Pearl's longest path analysis, please [click here](#) to read our article [Find and Analyze the Longest Combinational Paths, Meet Performance Goals](#).

For information on how Blue Pearl enables SoC RTL analysis, [click here](#) to read our white paper, [RTL analysis for complex FPGA designs using a Grey Cell methodology](#).

To register for ARM TechCon, please visit <https://armtechcon.reg.ubmelectronics.com>.

### About Blue Pearl Software

Blue Pearl Software, Inc. is a member of the [ARM Connected Community](#), and provides EDA software that accelerates RTL signoff for FPGA designs. The [Blue Pearl Software Suite](#) checks RTL designs for functional errors and automatically generates comprehensive and accurate Synopsys Design Constraints (SDCs) to improve Quality of Results (QoR) and reduce design risks.

Visit Blue Pearl Software at <http://www.bluepearlsoftware.com>.

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### Acronyms

CDC: Clock Domain Crossing  
EDA: Electronic Design Automation  
FPGA: Field Programmable Gate Array  
QoR: Quality of Results  
RTL: Register Transfer Level  
SDC: Synopsys Design Constraints  
SoC: System-on-Chip

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