Blue Pearl Software

NEWS
For Release April 06, 2012

Blue Pearl Software Names Roger Bitter VP of International Sales

New position addresses growing worldwide demand for EDA software that addresses the needs of FPGA designers

SANTA CLARA, California, USA–April 06, 2012 -Blue Pearl Software, Inc, a provider of next generation EDA software for FPGA and ASIC designers, announced that it has appointed Roger Bitter as Vice President of International Sales. Mr. Bitter will report to Paul Wilhelmsen, Vice President of Sales, and he will oversee international sales for the company's electronic design automation (EDA) software.

Blue Pearl Software Suite, for Windows and Linux operating systems, offers comprehensive RTL analysis, clock-domain crossing (CDC) checks, and automatic Synopsys Design Constraints (SDC) generation for FPGA, ASIC and SOC designs. Its visualization and validation technology gives users immediate feedback for validating automatically generated pre-synthesis longest paths and timing constraints.

"Roger has a long and successful track record growing markets for leading edge technology companies" stated Ellis Smith, CEO of Blue Pearl Software. "We look forward to his leadership as we continue to increase our international market penetration. He will help us address and the growing demand for our design analysis, clock domain crossing checking and timing constraint generation tools for FPGA and ASIC designs."

Mr. Bitter has over 30 years in sales and executive roles with software, semiconductor, and test products. Prior to Blue Pearl, he was VP Business Development at Mears Technologies Inc., a pioneer in the field of semiconductor Intellectual Property (IP). He also held various international

sales and operational functions at several technology companies, including Teseda Corporation, Xpedion Design Systems, Virage Logic, and Magma Design Automation. He holds an MBA in Finance, a MS in Management and a B.S. in Electronic Engineering.

Earlier this year, Blue Pearl Software announced Release 6.0 of its Blue Pearl Software Suite with capabilities that support FPGA designers, and support Synopsys' Synplify Pro® FPGA synthesis software. FPGA designers can learn more by visiting www.bluepearlsoftware.com/fpga/ and signing up for a hands-on workshops or software evaluation.

About Blue Pearl Software

Blue Pearl Software, Inc. focuses on solving the RTL analysis challenges designers face. Its Blue Pearl Software Suite offers automatically generated Synopsys Design Constraints (SDCs), lint and clock domain crossing (CDC) checking and an easy to use Visual Verification Environment™ to reduce the number of iterations required to close timing of multi-language (VHDL, SystemVerilog) designs. The software runs natively on Windows and Linux platforms, and is used for FPGA, ASIC and SOC design.

For the latest news and information on Blue Pearl Software, visit www.bluepearlsoftware.com.

###

Press Contact:
Georgia Marszalek, ValleyPR, LLC for Blue Pearl Software, +1-650.345.7477, Georgia@ValleyPR.com

Acronyms

ASIC: Application Specific Integrated Circuit
CDC: Clock Domain Crossing
EDA: Electronic Design Automation
FPGA: Field Programmable Gate Array
IP: Intellectual Property
RTL: Register Transfer Level
QoR: Quality of Results
SDC: Synopsys Design Constraints
SoC: System on Chip